SERVICE MANUAL FOR

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MiTAC

8599 N/B Maintenance

Contents

1. Hardware Engineering Specification …………………………………………… 4

1.1 Introduction …………………………………………… 4
1.2 Hardware System…………………………………………… 7
1.3 Electrical Characteristic …………………………………………… 37
1.4 Appendix 1 : SiS963L GPIO Definition …………………………………………… 42
1.5 Appendix 2 : Keyboard Controller Pins Definition …………………………………………… 43
1.6 Appendix 3: Audio Performance …………………………………………… 45

2. System View and Disassembly …………………………………………… 46

2.1 System View …………………………………………… 46
2.2 System Disassembly …………………………………………… 49

3. Definition & Location of Connectors / Switches …………………………………………… 69

3.1 Mother Board …………………………………………… 69

4. Definition & Location of Major Components …………………………………………… 72

4.1 Mother Board …………………………………………… 72

5. Pin Description of Major Component …………………………………………… 73

5.1 Inter Pentium 4 Processor mFC-PGA 478 Pins …………………………………………… 73
5.2 SiS M661FX (IGUI Host Memory Controller) …………………………………………… 78
5.3 SiS963L (MuTIOL®Media I/O South Bridge) …………………………………………… 83

8599 N/B Maintenance

Contents

6. System Block Diagram ………………………………………………………………………….. 89

7. Maintenance Diagnostics ………………………………………………………………….. 90

7.1 Introduction …………………………………………………………………………………… 90

7.2 Error Codes …………………………………………………………………………………… 91

7.3 Debug Tool ……………………………………………………………………………………… 93

8. Trouble Shooting ………………………………………………………………………………… 94

8.1 No Power ……………………………………………………………………………………….. 96

8.2 Battery Can not Be Charged ………………………………………………………………….. 99

8.3 No Display ……………………………………………………………………………………… 101

8.4 LCD No Display or Picture Abnormal ……………………………………………………….. 105

8.5 External Monitor No Display or Color Abnormal …………………………………………… 107

8.6 TV Test Error ………………………………………………………………………………….. 109

8.7 Memory Test Error ……………………………………………………………………………. 111

8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error ………………………………………………….. 113

8.9 Hard Driver Test Error ………………………………………………………………………….. 115

8.10 CD-ROM Driver Test Error …………………………………………………………………. 117

8.11 USB Port Test Error ………………………………………………………………………… 119

8.12 PC Card Socket Test Error ………………………………………………………………….. 123

8.13 Mini-PCI Socket Test Error ………………………………………………………………….. 125

8.14 Audio Failure ………………………………………………………………………………… 127

Contents

8.15 LAN Test Error ………………………………………………………………………………………… 130

9. Spare Parts List ……………………………………………………………………………………. 132

10. System Exploded Views …………………………………………………………………….. 143

11. Circuit Diagram ……………………………………………………………………………….. 144

12. Reference Material ……………………………………………………………………….. 172

8599 N/B Maintenance

1. Hardware Engineering Specification

1.1 Introduction

1.1.1 General Description

This document describes the system hardware engineer specification for 8599 portable notebook computer system.The 8599 notebook computer is a new mainstream high performance easy assembly notebook in the MiTAC notebook family.

1.1.2 System Overview (1)

Table 1. Hardware Specification

CPU	- Intel DT NW P4 2.4G,2.5G,2.53G,2.6G,2.66G,2.8G,3.06Ghz(p) w/z HT - FSB 800/533 MHz - Intel DT NW Celeron 2.0G~2.8G w/z - FSB 400MHz - Intel DT Prescott Celeron 2.4G,2.53G,2.66G,2.8G,3.06G,3.2G w/z - FSB 533MHz - Intel Northwood Mobile P4 2.40G,2.66G,2.80G,3.06G - Thermal ceiling 81.8W
Core logic	- SiS M661FX + SiS963L
L2 Cache	- 512KB OD for N/W DT & Mobile P4,128KB for N/W Celeron,256KB for Prescott Celeron
System BIOS	-Insyde 256KB(P) Flash EPROM (Include System BIOS and VGA BIOS) -ACPI 1.0b;DMI 2.3.1 compliant -Plug & Play capability

1.1.2 System Overview (2)

Continue to the previous page

Memory	- 0MB on board;Expandable up to 1024MB - Expandable with combination of optional 128MB/256MB/512MB memory - 184-pin DDR 266/333/400 DROM Memory Module x 2
ROM Drive	- 12.7mm Height - CD/DVD ROM Drive - Combo Drive - Super Combo Drive
HDD	- 2.5” 8.45/9.5 mm height:10/15/20/40GB - Support Ultra-DMA 66/100 function - User removable by latch,design reserve for screw fix
Ext.FDD	- Support External FDD w/z USB 1/F; 3.5” Format for 720KB/1.2MB/1.44MB
Display	- 15” XGA/TFT display; Resolution:1024x768
Video Controller	- SiS M661FX Int. w/64MB SMA
Keyboard	- 19mm key pitch/ 3.0mm key stroke/ 307mm length - Windows Logo Key x 1; Application Key x 1
Pointing Device	- Glide pad with 2x buttons and direction Scroll button
PCMCIA	- Type II x 1 without ZV - Cardbus Support
Indictor	- 3 LEDs for Power/battery/charge status (on display Housing/cover) - 1 LEDs for Radio wave status Power LED (BTO: Wireless LAN only) - 5 LEDs for HDD Access,ODD Access, Num lock, Cap lock and Scroll Lock

1.1.2 System Overview (3)

Continue to the previous page

Audio System	- Sound Blaster Pro compatible - Built-in mono microphone - AC97 2.2 Codec - 2X 2W Speakers
I/O Port	- USB port (2.0, backward compatible with USB 1.1) x 6 - RJ-11 port x 1 - RJ-45 port x 1 - DC input x 1 - VGA monitor port x 1 - Audio-out x 1 - Mic-in x 1 - S-Video TV-Out x 1 (NTSC/PAL)
Communication	- Built-in 56Kbps V.90 modem - Built-in 10/100 based-T LAN - One Mini-PCI slot and antenna reserved for wireless LAN
Battery	- 8 cell (2000mAH/3.7V) Li-ION smart battery
AC adapter	- Universal AC adapter 90W(P); Input: 100-240V,50/60hZ AC (support power on charge)
Dimensions	- 332x285x42 (max) (P)
Weight	- 3.5kg (P)

1.2 Hardware System

1.2.1 CPU Module

The Intel®Northwood DT Pentium®4 processor, Intel's most advanced, most powerful processor, is based on the new Intel®NetBurst™micro-architecture. The Pentium 4 processor is designed to deliver performance across applications and usages where end users can truly appreciate and experience the performance. These applications include Internet audio and streaming video,image processing, video content creation, speech, 3D, CAD, games, multi-media, and multi-tasking user environments. The Intel Northwood DT Pentium 4processor delivers this world-class performance for consumer enthusiast and business professional DT users as well as for entry-level workstation users.

Highlights of the Northwood DT Pentium 4 Processor:

- Available at speeds ranging from2.26G/2.4G/2.5G/ 2.53G/2.66G/2.8G/3.06G Hz
- Featuring the new Intel NetBurst™micro-architecture
- Fully compatible with existing Intel Architecture-based software
- Internet Streaming SIMD Extensions 2
- Intel®MMX™media enhancement technology
- Memory cache ability up to 4 GB of addressable memory space and system memory scalability up to 64GB of physical memory
- Support for uni-processor designs
- Based upon Intel's 0.13 micron manufacturing process

Intel Pentium 4 Processor Product Feature:

The Intel NetBurst™micro-architecture delivers a number of new and innovative features including Hyper Pipelined Technology, 400 or 533 MHz System Bus, Execution Trace Cache, and Rapid Execution Engine as well as a number of enhanced features Advanced Transfer Cache, Advanced Dynamic Execution, Enhanced Floating-point and Multi-media Unit, and Streaming SIMD Extensions 2. Many of these new innovations and advances were made possible with improvements in processor technology, process technology, and circuit design that could not previously be implemented in high-volume, manufacturability solutions. The features and resulting benefits of the new micro-architecture are defined below.

◆ Hyper Pipelined Technology

The hyper-pipelined technology of the NetBurst™micro-architecture doubles the pipeline depth compared to theP6 micro-architecture used on today's Pentium III processors. One of the key pipelines, the branch prediction / recovery pipeline, is implemented in 20 stages in the NetBurst™micro-architecture, compared to 10 stages in the P6 micro-architecture. This technology significantly increases the performance, frequency, and scalability of the processor.

◆ 400/533 MHz System Bus:

The Northwood DT Pentium 4 processor supports Intel's highest performance desktop system bus by delivering 3.2 or 4.3GBof data per second into and out of the processor. This is accomplished through a physical signaling scheme of quad pumping the data transfers over a100/133-MHz clocked system bus and a buffering scheme allowing for sustained 400/533-MHz data transfers. This compares to 1.06 GB/s delivered on the Pentium III processor's 133-MHz system bus.

Level 1 Execution Trace Cache:

In addition to the 8KB data cache, the Pentium 4 processor includes an Execution Trace Cache that stores up to12K decoded micro-ops in the order of program execution. This increases performance by removing the decoder from the main execution loop and makes more efficient usage of the cache storage space since instructions that are branched around are not stored. The result is a means to deliver a high volume of instructions to the processor's execution units and a reduction in the overall time required to recover from branches that have been mis-predicted.

Rapid Execution Engine:

Two Arithmetic Logic Units (ALUs) on the Pentium 4 processor are clocked at twice the core processor frequency. This allows basic integer instructions such as Add, Subtract, Logical AND,Logical OR, etc. to execute in half a clock cycle. For example, the Rapid Execution Engine on a 1.50 GHz Pentium 4 processor runs at 3 GHz.

512KB, Level 2 Advanced Transfer Cache:

The Level 2 Advanced Transfer Cache (ATC) is 512KB in size and delivers a much higher data throughput channel between the Level 2 cache and the processor core. The Advanced Transfer Cache consists of a 256-bit(32-byte) interface that transfers data on each core clock. As a result,the Northwood DT Pentium 4 processor 1.6 GHz can deliver a data transfer rate of 48 GB/s.This compares to a transfer rate of 16 GB/s on the Pentium III processor at 1 GHz. Features of the ATC include:

- Non-Blocking, full speed, on-die Level 2 cache
- 8-way set associativity

- 256-bit data bus to the level 2 cache
- Data clocked into and out of the cache every clock cycle

◆ **Advanced Dynamic Execution:**

The Advanced Dynamic Execution engine is a very deep, out-of-order speculative execution engine that keeps the execution units executing instructions. The Pentium 4 processor can also view 126 instructions in flight and handle up to 48 loads and 24 stores in the pipeline. It also includes an enhanced branch prediction algorithm that has the net effect of reducing the number of branch mis-predictions by about 33% over the P6 generation processor's branch prediction capability. It does this by implementing a 4KB branch target buffer that stores more detail on the history of past branches, as well as by implementing a more advanced branch prediction algorithm.

◆ **Enhanced Floating-Point and Multimedia Unit:**

The Pentium 4 processor expands the floating-point registers to a full 128-bit and adds an additional register for data movement which improves performance on both floating-point and multimedia applications..

◆ **Internet Streaming SIMD Extensions 2 (SSE2):**

With the introduction of SSE2, the NetBurst™micro-architecture now extends the SIMD capabilities that MMX technology and SSE technology delivered by adding 144 new instructions. These instructions include 128-bit SIMD integer arithmetic and 128-bit SIMD double-precision floating-point operations. These new instructions reduce the overall number of instructions required to execute a particular program task and as a result can contribute to an overall performance increase. They accelerate a broad range of applications, including video, speech,and image, photo processing, encryption, financial,engineering and scientific applications.

◆ **Features Used for Test and Performance / Thermal Monitoring:**

- Built-in Self Test (BIST) provides single stuck-at fault coverage of the microcode and large logic arrays, as well as testing of the instruction cache, data cache, Translation Look aside Buffers (TLBs), and ROMs.
- IEEE 1149.1 Standard Test Access Port and Boundary Scan mechanism enables testing of the Pentium 4 processor and system connections through a standard interface.
- Internal performance counters can be used for performance monitoring and event counting.
- Includes a new Thermal Monitor feature that allows motherboards to be cost effectively designed to expected application power usages rather than theoretical maximums.

1.2.2 SiS M661FX Graphics/Memory Controller

The SiSM661FX chipset features a SiS Real256E GPU, an AGP-8X port, and a Shared Memory Architecture DDR400 unified memory controller, supporting Intel Hyper Threading Technology Pentium 4 microprocessors series with FSB 800MHZ. The integrated Real256E GPU features a high performance 3D / 2D Graphics engine, a video accelerator, a MPEG1/II motion compensation decoder, and a video link(Muxed with AGP port) to support the TV-out & digital flat panel. The SiSM661FX, adopting the SMA, eliminates the need and thus the cost of the frame buffer memory by organizing the frame buffer,32MB or 64MB, in the system memory. The SiSM661FX, via the second-generation 1GB/s Multi-threaded I/O link, interconnects the SiS963 Media I/O that integrates one EHCI compliant USB2.0 host controller, 2 OHCI compliant USB 1.1 host controllers, dual ATA-133 IDE controllers, AC-97 V2.2 compliant audio controller, and the 10/100M bit Ethernet MAC controller with standard MII interface. Figure 1 illustrates a Pentium 4 PC system diagrams based on SiSM661FX and SiS963 chipsets.

The SiSM661FX Host Interface features the AGTL & AGTL+ compliant bus driver technology with integrated on-die termination to support Intel Pentium 4 series processors with FSB 800MHz. The AGP interface supports the external AGP slot with AGP 4X/8X capability and Fast Write Transactions. The SiSM661FX incorporates the second generation 1GB/s MuTIOL1G interface, comprising the transaction layer, link layer, and physical layer, to bridge the SiS963 Media I/O. As seen in table 1, the SiSM661FX comprises two PCI devices sitting on the bus 0, and one PCI device on the Bus 1.The device 0 stands for the SiSM661FX entity with device ID 0661h, and IDSEL equal to AD11. The device 1 functions a virtual PCI to PCI bridge to connect the AGP device, with device ID equal to 0002h, and IDSEL equal to AD12. The device 0 in the bus 1 represents the integrated Real256E GPU, with device ID equal to 6330h. The integrated GUI device 6330h cannot work concurrently with an external AGP graphics device. When an external AGP device is installed in the system, the built-in GUI will be disabled. Figure 2 illustrates a graphic subsystem based on the integrated GUI in SiSM661FX.

The integrated Real256E GPU features a high performance 3D accelerator with 2 Pixel / 4 Texture, and a 128 bit 2D accelerator with 1T pipeline BITBLT engine. Two 12 bit DDR digital video links interfaced to SiS 301/2 Video Bridge is incorporated to expand the SiSM661FX functionality to support the secondary display, in addition to the default primary CRT display. The SiS301 Video Bridge features an NTSC/PAL video encoder with Macro Vision Ver. 7.1.L1 option for TV display, a TMDS transmitter with Bi-linear scaling capability to support up to UXGA TFT LCD panel, and an analog RGB port to support the secondary CRT. The primary CRT display and the extended secondary display, namely TV, TFT LCD, or 2'nd CRT, features the Dual Display Capability in the sense that both can generate the display in independent resolutions, color depths, and frame rates. Table 2 details the capability of the video overlay capability in SiSM661FX+SiS301/302 subsystem. In a summary, in the mirror mode, two separate H/W video overlay engines, and two separate subpicture engines work simultaneously to deliver high quality video overlay with subpicture in the respective display consoles simultaneously, say in the LCD, and CRT for the presentation application. However, in the dual display mode, only one H/W video overlay, and one subpicture engine can be enabled to overlay the video display and the subpicture in one display while the support of the second video overlay with subpicture in.

the second display can only be realized through software engine.

Two separate buses, the 64 bit Host-to-GUI bus, and the 128 bit IGUI-to-Memory Controller bus are devised to ensure concurrency of Host-to-GUI, and GUI-to-MC streaming. In the DDR-400 memory subsystem, the 128 bit IGUI-to-MC bus attains 3.2 GB/s, around 52% wider bandwidth than the AGP 8X one. The DDR-400 unified memory controller mainly comprises the Memory Arbiter, the M-data/M-Command Queues, and the Memory Interface. The Memory Arbiter arbitrates a plenty of memory access requests from the GUI or AGP controller, Host Controller, and the I/O bus masters based a default optimized priority list with the capability of dynamically prioritizing the I/O bus master requests to offer a privileged service to 1) the isochronous downstream transfer to guarantee the min. latency, & timely deliver, or 2) the PCI master downstream transfer to curb the latency within the max. tolerant period of 10us. Prior to the memory access requests pushed into the M-data queue, any command complaint to the paging mechanism is generated and pushed into the M-CMD queue. The M-data/M-CMD queue further orders and forwards these queuing requests to the Memory Interface in an effort to utilizing the memory bandwidth to its utmost by scheduling the command requests in the background when the data request streamlines in the foreground.

Features :

- **PC2001 Compliance**
- **High Performance Host Interface**

  - Supports Intel Pentium 4 processor family with data transfer rate
  - Supports Hyper-Threading Technology
  - Supports 12 outstanding transactions and out-of-order completion
  - Supports Quasi-synchronous/asynchronous Host-to-DRAM timing
  - Supports Master delivery System bus Interrupt

8599 N/B Maintenance

- Supports zero-wait state for contiguous CPU write data
- Supports 128K/256K/512K/1M/2M/4M/8M/16M TSEG SMRAM
- Supports Defer Function to maximize bus utilization
- Supports Dynamic Bus Inversion
- AGTL+ & AGTL compliant bus driver with auto compensation

- **64 Bit High Performance DDR400/DDR333/DDR266 Memory Controller**

  - Supports DDR400/DDR333/DDR266 SDRAM
  - Supports up to 2 un-buffered DIMM DDR400
  - Supports up to 3 un-buffered DIMM DDR333
  - Up to 1 GB per DIMM with maximum memory size up to 3 GB
  - Supports 32Mb, 64Mb, 128Mb, 256Mb, 512Mb, 1Gb SDRAM technology with page size from 2KB up to 32 KB
  - Supports up to 24 open pages
  - Sustains DDR SDRAM CAS Latency at options of 2, 2.5, & 3 clocks
  - Auto-compensation SSTL-2.5v driver optimizing for performance and stability
  - Supports Suspend to DRAM function
  - Programmable shared frame buffer size 32MB or 64MB for display memory
  - 128KB SMRAM space re-mapping to A0000h, B0000h, or E0000h

- **Integrated A.G.P. Compliant Target/66MHz Host-to-PCI Bridge**

  - Universal AGP v3.0 Compliant
  - Support 1.5V AGP Interface Only

8599 N/B Maintenance

- Supports Graphic Window Size from 4MBytes to 512MBytes
- Supports Pipelined Process in CPU-to-A.G.P. Access
- Supports 8 Way, 16 Entries Page Table Cache for GART to Enhance A.G.P. Controller Read/Write Performance
- Supports PCI-to-PCI Bridge Function for Memory Write from 33Mhz PCI Bus to A.G.P. device
- Supports AGP 8X/4X Interface w/ Fast Write Transaction
- Supports Hardware Enforced Coherence Outside GART Range for A.G.P. Transaction
- Supports Data Bus Inversion and Calibration Cycle

High Throughput SiS MuTIOL® 1G Interconnecting to SiS963 MuTIOL 1G Media I/O

- Bi-directional 16 bit data bus
- Perform 1GB/s bandwidth in 133MHz x 4 mode
- Distributed arbitration strategy with long contiguous data streaming
- Packet based, pipelining, and split transaction scheme

Dedicated Isochronous Response Queue

- Priority promotion for upstream Isochronous DMA memory read requests originated from real-time I/O device controllers, such as USB or audio/modem
- Dedicated Isochronous response queue serving Isochronous downstream transfers responsive to the memory read requests originated from real-time I/O device controllers, such as USB or audio/modem. Offers privilege service to guarantee minimum latency & timely delivery

High Performance & High Quality 3D Graphics Accelerator

- Built-in a high performance 256-bit 3D engine

8599 N/B Maintenance

- -- Built-in 32-bit floating point format VLIW triangle setup engine
- -- Built-in 2 pixel rendering pipelines and 4 texture units
- -- Built-in hardware stereo auto rendering engine
- -- Supports Ultra-AGPIITM up to 2.7GB/s bandwidth
- -- Up to 133 MHz 3D engine clock speed
- -- Peak polygon rate: 11.6 M polygon/sec @ 1 pixel/polygon with Gouraud shaded, point-sampled, linear and bilinear texture mapping
- -- Peak fill rate: 333 M pixel/sec, 666 M texture/sec @ 10,000 pixel/polygon with Gouraud shaded and two bilinear textured, Z buffered and alpha blended

- Built-in a high quality 3D engine
  - -- Supports flat, and Gouraud shading
  - -- Supports high quality dithering
  - -- Supports Z-test, stencil test, Alpha-test, and scissors clipping test
  - -- Supports 16 ROPs
  - -- Supports Z-buffer, stencil buffer
  - -- Supports 16/24/32 bits integer Z buffer format and 32 bits floating point Z format
  - -- Supports 16/32 BPP render buffer format
  - -- Supports 1/2/4/8 stencil buffer format
  - -- Supports per-pixel texture perspective correction
  - -- Supports point-sampled, linear, bi-linear, and dual bi-linear texture filtering
  - -- Supports up to 2 pixels with 4 bi-linear texels within single cycles
  - -- Supports up to 2048x2048 texture size
  - -- Supports rectangle structure texture

-- Supports 16/24/32 bpp RGB/ARGB texture format
-- Supports DTX1, DTX2, DTX3 texture compression formats
-- Supports texture transparency, blending, wrapping, mirror, and clamping
-- Supports fogging, alpha blending
-- Supports vertex fogging and fog table
-- Supports specular lighting
-- Supports 2X/4X multi-sampling full scene anti-aliasing
-- Supports back face culling
-- Supports auto-stereo rendering

- **High Performance 2D Graphics Accelerator**

- Built-in hardware command queue
- Built-in Direct Draw Accelerator
- Built-in GDI 2000 Accelerator
- Built-in an 1T pipelined 128-bit BITBLT graphics engine with the following functions:

-- 256 raster operations
-- Rectangle fill
-- Trapezoid fill
-- Color expansion
-- Enhanced color expansion
-- Line-drawing with styled pattern
-- NT fractional point line-drawing with styled pattern
-- Multiple scan line

  - -- Built-in 256 bytes pattern registers
  - -- Built-in 8x8 mask registers
  - -- Rectangle clipping
  - -- Transparent BitBlt with source and destination keys (16 ROPs)
  - -- Gradient color fill
  - -- Anti-aliasing text drawing
  - -- Alpha blended Bitblt
  - -- YUV to RGB color transform Bitblt
  - -- Source data in command queue Bitbl
  - -- YUV420 to YUV422 format conversion Bitblt
- Supports memory-mapped, zero wait-state, burst engine write
- Built-in 64x64x2 bit-mapped mono hardware cursor
- Built-in 64x64x16 bit-mapped blended color hardware cursor
- Maximum 128MB frame buffer with linear addressing
- Built-in engine write-buffer with byte-merge
- Supports Ultra-AGPIITM 2.7GB/s for DDR333 and 3.2GB/s for DDR400 data read for all 2D Graphics engine functions
- Built-in source read-buffer to minimize engine wait-state
- Built-in destination read-buffer to minimize engine wait-state

Complete TV-OUT/Digital Flat Panel Solution

- Built-in secondary CRT controller to support independent display of secondary CRT, LCD and TV-out

- AGP signals multiplexed with two 165MHz dot clock 12-bit DDR digital video link connecting to SiS video bridge (SiS301, and SiS302) supporting
    - -- NTSC/PAL video output with max. resolution 1024x768x32@60NI
    - -- Digital LCD monitor with max. resolution 1600x1200x32@60NI
    - -- The secondary CRT with max. resolution 1600x1200x32@60NI
    - -- The Independent dual view support of the CRT+LCD, CRT+TV, LCD+TV combinations.

MPG-2/1 Video Decoder

- MPEG-2 ISO/IEC 13818-2 MP@HL and MPEG-1 ISO/IEC 11172-2 standards compliant
- Built-in advanced hardware DVD acceleration logic
- Support AGP bus master/LFB-mode code fetching
- Half pixel resolution in motion compensation
- Supports up to 20 Mbit/sec bit rate decoding
- Support VCD, DVD and HDTV (all ATSC modes) decoding
- Direct DVD to TV playback

Video Accelerator

- Supports video windows with overlay function
- Supports YUV-to-RGB color space conversion
- Supports bi-linear video interpolation with integer increments of 1/2048
- Supports graphics and video overlay function
    - -- Independent graphics and video formats

- -- 16 color-key and/or chroma-key operations
- -- Support YUV or RGB format chroma key
- -- Rectangular video window mode
- -- Video only mode
- -- VCD, DVD and up to HDTV playback mode
- -- Supports reading-back of current refresh scan line

- Supports tearing free double buffer flipping
- Supports RGB555, RGB565, YUV422, and YUV420 video playback format
- Supports filtered horizontal up and down scaling playback
- Supports de-interlaced function to improve field-display sources display quality
- Supports DVD sub-picture playback overlay
- Supports DVD playback auto-flipping
- Built-in video playback line buffers to support 1920x1080 video playback
- Supports DVD sub-picture playback overlay
- Built-in video line buffers and sub-picture buffers for DVD quality video
- Built-in independent Gamma correction RAM
- Supports DCI Drivers
- Supports Direct Draw Drivers

High Integration

- Built-in CRT FIFOs to support ultra high resolution graphics modes and reduce CPU wait-state
- Built-in programmable 24-bit true-color RAMDAC up to 333 MHz pixel clock

8599 N/B Maintenance

  - -- Built-in reference voltage generator and monitor sense circuit
  - -- Supports downloadable 24 bits RAMDAC for gamma correction in high color and true color modes
  - -- Support programmable 4 levels DAC current ratio (700, 750, 800, 850 mv)
  - -- Support programmable pedestal level (0, 0.75mv)
  - -- Support programmable 4 levels slew rate control
- - Built-in two clock generators for CRT, 2D, 3D and MPEG Engine
- - Built-in TV Encoder Interface

- **Power Management**

  - - Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management
  - - Supports direct I/O command to force graphics controller into standby/suspend/off state
  - - Power down internal Gamma/Palette SRAM in direct color mode
  - - Supports PCI power management configuration registers for supporting ACPI power down controller
  - - Power down all internal macro cells such as SRAM, DAC, clock generator when power saving mode
  - - Supports clock stopping for video accelerator, 2D, 3D and MPEG decoder when disabled
  - - Supports auto clock throttling for 2D engine, 3D engine

1.2.3 SiS963L MuTIOL 1G Media I/O

The SiS963L MuTIOL 1G Media I/O integrates one Universal Serial Bus 2.0 Host Controllers, the Audio Controller with AC 97 Interface, the Ethernet MAC Controller w/ standard MII interface, two Universal Serial Bus 1.1 Host Controllers, the IDE Master/Slave controllers, and SiS MuTIOL 1G technology. The PCI to LPC bridge, I/O Advanced Programmable Interrupt Controller, legacy system I/O and legacy power management functionalities are integrated as well.

The high-speed host controller implements an EHCI compliant interface that provides 480Mb/s bandwidth for six USB 2.0 ports. The two USB1.1 host controllers implement an OHCI compliant interface and each USB1.1 host controller provides 12Mb/s bandwidth for three USB 1.1 ports. The totally six USB ports can be automatically routed to support a High-speed USB 2.0 device or Full- or Low-speed USB 1.1 device. Besides, each port can be optionally configured as the wake-up source. Legacy USB devices as well as over current detection are also implemented. The Integrated AC97 v2.2 compliance Audio Controller that features a 6-channels of audio speaker out and HSP v.90 modem support. Additionally, the AC97 interface supports 4 separate SDATAIN pins that is capable of supporting multiple audio codecs with one separate modem codec.

The integrated Fast Ethernet MAC Controller features an IEEE 802.3 and IEEE 802.3x compliant MAC with external LAN physical layer chip supporting full duplex 10 Base-T, 100 Base-T Ethernet, or with external Home networking physical layer chip supporting 1Mb/s & 10Mb/s Home networking. Additionally, 5 wake-up Frames, Magic Packet and link status changed wake-up function in G1/G2 states are supported. For storing Mac address, two schemes are provided: 1. Store in internal APC register or 2. Store in external EEPROM.

The integrated IDE Master/Slave controllers features Dual Independent IDE channels supporting PIO mode 0,1,2,3,4, and Ultra DMA 33/66/100/133. It provides two separate data paths for the dual IDE channels that sustain the high data transfer rate in the multitasking environment.

SiS963L supports 6 PCI masters and complies with PCI 2.2 specification. It also incorporates the legacy system I/O like: two 8237A compatible DMA controllers, three 8254 compatible programmable 16-bit counters, hardwired keyboard controller and PS2 mouse interface, Real Time clock with 512B CMOS SRAM and two 8259A compatible Interrupt controllers. Besides, the I/O APIC managing up to 24 interrupts with both Serial and FSB interrupt delivery modes is supported.

The integrated power management module incorporates the ACPI 1.0b compliance functions, the APM 1.2 compliance functions, and the PCI bus power management interface spec. v1.1. Numerous power-up events and power down events are also supported. 25 general purposed I/O pins are provided to give an easy to use logic for specific application. In addition, the SiS963L supports Deeper Sleep power state for Intel Mobile processor. For AMD processor, the SiS963L use the CPUSTP# signal to reduce processor voltage during C3 and S1 state.

A high bandwidth and mature SiS MuTIOL 1G technology is incorporated to connect SiS MuTIOL 1G North Bridge and SiS963L MuTIOL1G Media I/O together. SiS MuTIOL 1G technology is developed into three layers, the Multi-threaded I/O Channels Layer delivering 1.2GB bandwidth to connect embedded DMA Master devices and external PCI masters to interface to Multi-threaded I/O Channels layer, the Multi-threaded I/O Packet Layer in SiS963L to transfer data w/ 1GB/s bandwidth from/to Multi-threaded I/O Channels layer to/from SiS MuTIOL 1G North Bridge, and the Multi-threaded I/O Packet Layer in SiS MuTIOL 1G North Bridge to transfer data w/ 1GB/s from/to memory sub-system to/from the Multi-threaded I/O Packet Layer in SiS963L.

8599 N/B Maintenance

Features :

- **Meet PC2001 Requirements**
- **Support AMD Hammer CPU and HyperTransport Technology.**
- **Support Watchdog Timer Hardware Requirements for Microsoft Windows .NET Server**
- **High performance SiS MuTIOL 1G Technology Interconnecting SiS North bridge and South bridge chips**
  - Bi-directional 16-bit data bus
  - Perform 1GB/s bandwidth in 133MHz x 4 mode
  - Distributed arbitration strategy with long contiguous data streaming
  - Packet based, pipelining, and split transaction scheme
- **Integrated Multi-threaded I/O link ensures concurrency of upstream/down stream data transfer with1.2GB/s bandwidth**
- **Multiple DMA Bus Architecture**
  - Concurrent Servicing of all DMA Devices: Dual IDE Controllers, two USB 1.1 HC, One USB 2.0 HC, MAC Controller, Audio/Modem DMA Controller
  - Separate 32 Bit Input and Output Data Bus Scheme for each DMA Device
  - Advanced Performance Merits of Split & Pipelined Transaction and Concurrent
  - Execution among Multi-I/O Devices
  - Support isochronous request and continuous packet transmission

8599 N/B Maintenance

- **Integrated MuTIOL 1G to PCI Bridge**
  - PCI 2.2 Specification Compliance
  - Supports up to 6 PCI Masters
  - Two Prefetch cache Buffers support 2 delayed transactions
  - Each PCI request can be programmed at one of four level priority
  - Write Promotion Mechanism to Guarantee the 10 µs Time Limit of PCI Memory Write
- **Dual IDE Master/Slave Controller**
  - Integrated Multithreaded I/O Link Mastering with Read Pipelined Streaming
  - Dual Independent IDE Channels Each with 32 DW FIFO
  - Native and Compatibility Mode
  - PIO Mode 0, 1, 2, 3, 4 and Multiword DMA Mode 0, 1, 2
  - Ultra DMA 33/66/100/133
  - ATA/ATAPI 48-bit addressing compliance and support greater than 137Gbytes device.
  - Silicon Integrated Series Termination Resistors
  - Silicon Integrated IDE Bus pull up / down resistors
  - PCI 2.2 Specification Compliance
  - Bus master programming interface (SFF-8038i) specification compliance
- **Universal Serial Bus Host Controller**
  - Integrated Multithreaded IO Link Mastering
  - Two Independent OHCI USB 1.1 Host Controllers and One EHCI USB 2.0 Host Controller, support up to six ports

- Supports wake-up from S1-S3
- Legacy Keyboard/Mouse support
- Supports only one Debug port at port 0(first port), it is at USB 2.0 transfer rate.

- **Integrated Fast Ethernet MAC Controller**
  - Multithread I/O link Mastering with Read/Write Concurrent transaction
  - IEEE 802.3 and 802.3x Standard Compatible
  - Supports Enhanced Software and Automatic Polling schemes to access PHY registers
  - Supports full duplex 10base-T, 100base-Tx, 1 Mb/s & 10 Mb/s Home Networking
  - Support ACPI v1.0b and PCI Power Management v1.1 Standard
  - Support 5 Wake-up Frame, Magic Packet, and Link Status changed wake-up function at G1/G2 state
  - Integrated 128-bit multicast hash table
  - Support 2K bytes transmit and receive Data FIFO
  - MAC address store scheme from external 4-pin EEPROM or Internal APC register

- **Integrated Audio Controller with AC97 Interface.**
  - AC97 v2.2 compliance
  - 6 Channels of AC97 speaker outputs and V.90 HSP-Modem
  - 4 Separate SDATAIN pins supporting multiple Audio Codecs and one Modem Codec
  - Supports Audio and Modem function with Multithreaded I/O link mastering
  - Supports two Consumer Audio Digital interface: traditional Consumer Digital Audio Out and AC97 V2.2 Compliance Consumer Audio Digital Interface

- Supports VRA Mode for both AC97 Audio Link and Consumer Audio Digital Interface

- **Advanced Power Management**
  - Meets ACPI 1.0b Requirements
  - Meets APM 1.2 Requirements
  - ACPI Sleep States Include S1, S3, S4, S5
  - CPU Power States Include C0, C1, C2 C3, C4
  - Supports Intel Deeper Sleep Power State for Intel mobile processor.
  - Reduce AMD processor voltage during S1/C3 state
  - Power Button with Override only wake up by Power Button
  - RTC Day-of-Month, Month-of-Year Alarm
  - 24-bit Power Management Timer
  - LED Blinking in S0, S1 and S3 States
  - ACPI System Wake-up Events
  - ACPI S1 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-key and Mouse, RTC Alarm, Modem, Ring-In, LAN, PME#, AC’97 Wake-Up, USB Wake-Up, and 1394 Wake-up
  - ACPI S3 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-key and Mouse, RTC Alarm, Modem, Ring-In, GPIO7, LAN, PME#, AC’97 Wake-Up, USB Wake-Up, and 1394 Wake-up.
  - ACPI S4/S5 Wake-up Events: Power Button, PS/2 keyboard Hot-Key/Any-Key and Mouse, RTC Alarm, Modem, Ring-In, GPIO7, LAN, PME#, AC’97 Wake-Up, and P1394 Wake-up.
  - Software Watchdog Timer
  - PCI Bus Power Management Interface Spec. 1.1

8599 N/B Maintenance

- Support PCI CLKRUN and STP_PCI function (for Mobile only)
- Support RTC32KHz output from GPIO18 (for Mobile only)
- Integrated 32-bit Random Number Generator
- Support one GTL-level input signal used to instantly power off the system
- Support one GTL-level input signal used to assert SMI#/SCI#

- **Integrated DMA Controller**
  - Two 8237A Compatible DMA Controllers
  - 8/16- bit DMA Data Transfer

- **Integrated Interrupt Controller**
  - Two 8259A Compatible Interrupt Controllers for up to 15 interrupts
  - Programmable Level or Edge Triggered Interrupts
  - Support Serial Interrupt
  - Support 8 PCI interrupts for internal device
  - Support Message Interrupt Delivery Mode
  - Integrated I/O APIC in Serial Mode or FSB Interrupt Delivery Model for up to 24 Interrupts

- **Three 8254 Compatible Programmable 16-bit Counters**
  - System Timer Interrupt
  - Generate Refresh Request
  - Speaker Tone Output

8599 N/B Maintenance

- **Integrated Keyboard Controller**
  - Hardwired Logic Provides Instant Response
  - Supports PS/2 Mouse Interface
  - System Sleep and Power-Up by Hot-Key
  - KBC and PS2 Mouse Can Be Individually Disabled
- **Integrated High-Performance Event Timer**
  - Support three timers operating at 32- or 64-bit mode
- **Integrated PCI to LPC Bridge**
  - LPC 1.0 Compliance
  - Support Two Master/DMA devices
- **Integrated Real Time Clock (RTC) with 512B CMOS SRAM**
  - Supports ACPI Day-of-Month and Month-of-Year Alarm
- **Universal Serial Bus Host Controller**
- **NAND Tree for Ball Connectivity Testing**
- **371-Balls BGA Package**
- **1.8V Core with Mixed 1.5V, 1.8V, 2.65V and 3.3V I/O CMOS Technology**

1.2.4 Memory

- 64MB 400/33/266MHz DIMM DDR Memory expandable to 1024 MB (2 DDR slot)
- Support 184pin DDR DIMM Memory

Table 2. Memory Expansion Capacity

Slot1	Slot2	Slot3
256MB	0MB	256MB
256MB	256MB	512MB
512MB	0MB	512MB
512MB	256MB	768MB
512MB	512MB	1024MB

1.2.5 I/O Ports

- **Audio Ports**

  - Microphone In & Line Out

  - Built in 2 high quality internal speaker (2W)

  - Built in 1 mono microphone

RJ-11

- Connection to Modem Daughter Board Connector

Table 3. Modem Port

Pin	Signal Name	Direction	Description
1	NC	-	No Connect
2	LINE +	I/O	Phone Line Positive
3	LINE -	I/O	Phone Line Negative
4	NC	-	No Connect

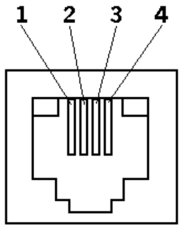


Figure 1 . Modem Connector

RJ-45

- Connection to On-Board NIC controller

Table 4. LAN Port

Pin	Signal Name	Direction	Description
1	TX+	Out	Transmit Data Ring
2	TX-	Out	Transmit Data Tip
3	RX+	IN	Receive Data Ring
4	TERM1	-	Internal termination resistor
5	TERM2	-	Internal termination resistor
6	RX	IN	Receive Data Tip
7	TERM3	-	Internal termination resistor
8	TERM4	-	Internal termination resistor

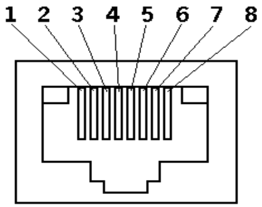


Figure 2 . LAN Connector

USB Ports

- Six industry standard USB 2.0 ports

Table 5. USB Port

Pin	Signal Name	Direction	Description
1	VCC	-	USB Device Power (+5VDC)
2	DATA-	I/O	Balanced Data Negative
3	DATA+	I/O	Balanced Data Positive
4	GND	-	Ground

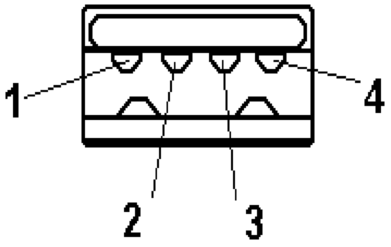


Figure 3 . USB Connector

7 Pins S-VIDEO Port for TV-Out

- Support up 1024*768 resolution

- Support PAL and NTSC system

- Support composite Output by a transfer cable(RCA)

Table 6. S-Video Port

Pin	Signal Name	Direction
1	GND	-
2	NC	-
3	GND	-
4	LUMA	O
5	NC	-
6	CRMA	O
7	COMP	O

CRT Ports

- Standard VGA compatible port
- DDC1 and DDC2B compliant (RCA)

Table 7. CRT Connector

PIN	SIGNAL	DESCRIPTION
1	RED	Red analog video output
2	GREEN	Green analog video output
3	BLUE	Blue analog video output
4	Monitor Sense	Monitor Sense
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	VCC	+5VDC
10	GND	Ground
11	Monitor Sense	Monitor Sense
12	CRT DATA	Data from DDC monitor
13	HSYNC	Horizontal Sync control
14	VSYNC	Vertical Sync control
15	CRT CLK	Clock to DDC monitor

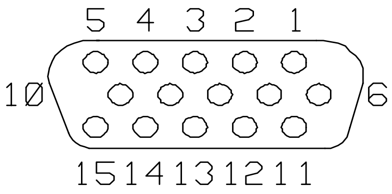


Figure 4 . CRT Connector

1.2.6 PC Card Slot

- One Type II/I slot supporting the 1997 PC Card standard,and including full R2 (16-bit) and 32-bit Cardbus data transfer
- TI PCI1410A (PCMCIA Controller) & TI TPS2211A (Power Switch)

1.2.7 Graphical Subsystem

- Integrate Real256E GPU +SIS301LV Video Bridge

1.2.8 Display

- Internal LCD Display is 15” TFT XGA panel
- External Video refresh rate of up to 85Hz supported

  - Vertical refresh frequencies to meet VESA requirements
  - Simultaneous video in specified video modes – switchable with hot key

1.2.9 LEDs Indiactor

- CDROM & HDD & NUM & CAP & SCROLL & WLAN
- AC & BAT & CHARGE

1.2.10 Read Only Memory (BIOS Flash)

- Fully compatible with industry standard software including Windows 2000 & Windows XP
- Fully supports APM V1.2 and latest ACPI specification
- 2Mb Flash BIOS
- Inside BIOS core

1.2.11 Power Management Features

- Local standby mode (Individual devices such as HDD, graphics controller,LCD etc..)
- CPU Idle mode (Including ACPI modes C1 and C2)
- Suspend mode (Including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant
- Fully ACPI V1.1 compliant
- Hibernate for Windows XP
- Thermal management
- Fully US EPA Energy Start compliant

1.2.12 Keyboard Controller

- Winboard W83L950D

1.2.13 Buttons

- Power on bin

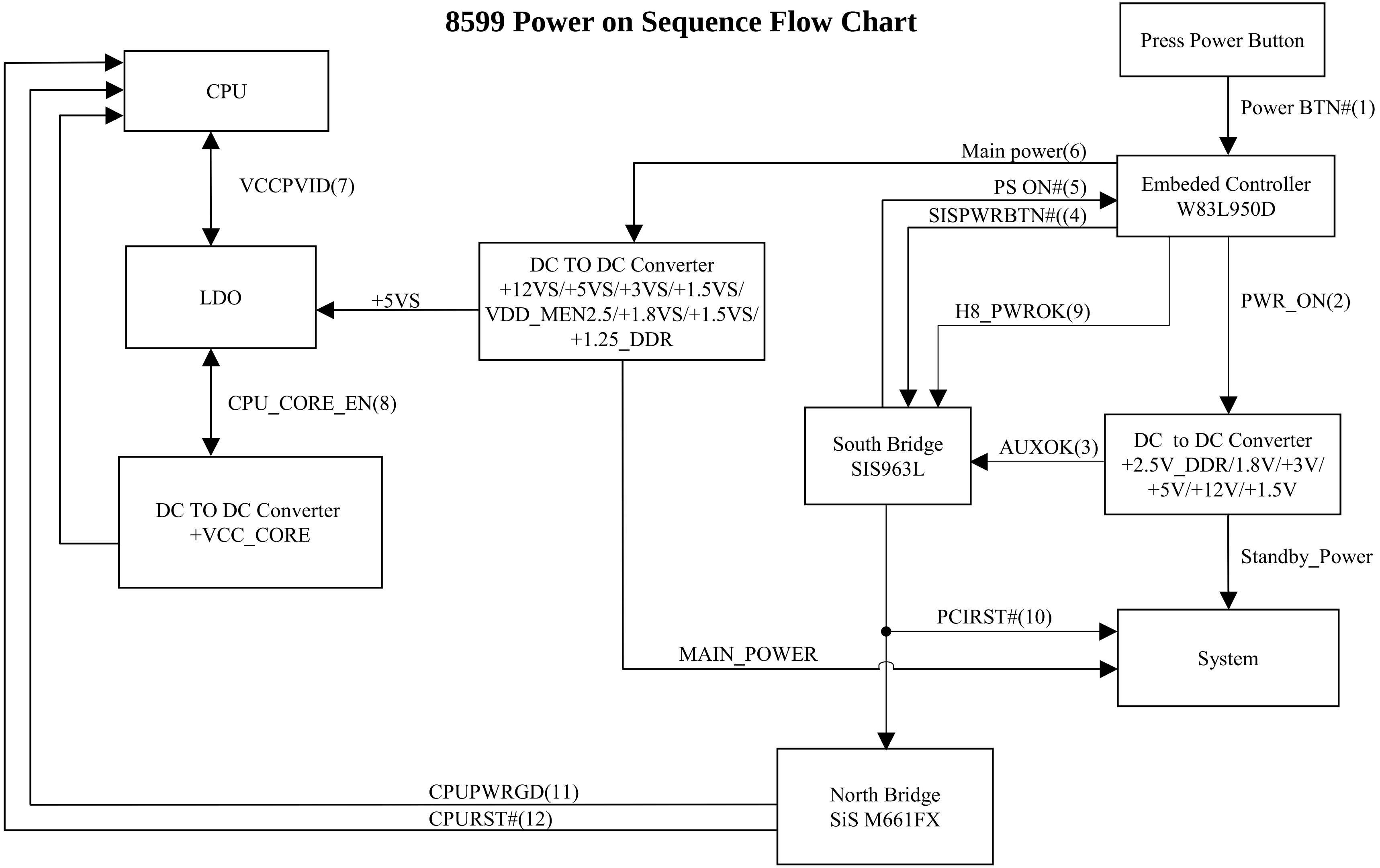
1.2.14 Modem

Table 8. Modem Daughter Board Connector

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	MONO_OUT	2	NC
3	GND	4	MODEM_SPK
5	NC	6	NC
7	NC	8	GND
9	NC	10	+5V
11	NC	12	NC
13	NC	14	NC
15	GND	16	Pull Up to +3V
17	+3V	18	+5V
19	GND	20	GND
21	+3V	22	ACSYNC
23	ACSDOUT	24	MSDIN
25	-ACRST	26	MSDIN
27	GND	28	GND
29	GND	30	ACBITCLK

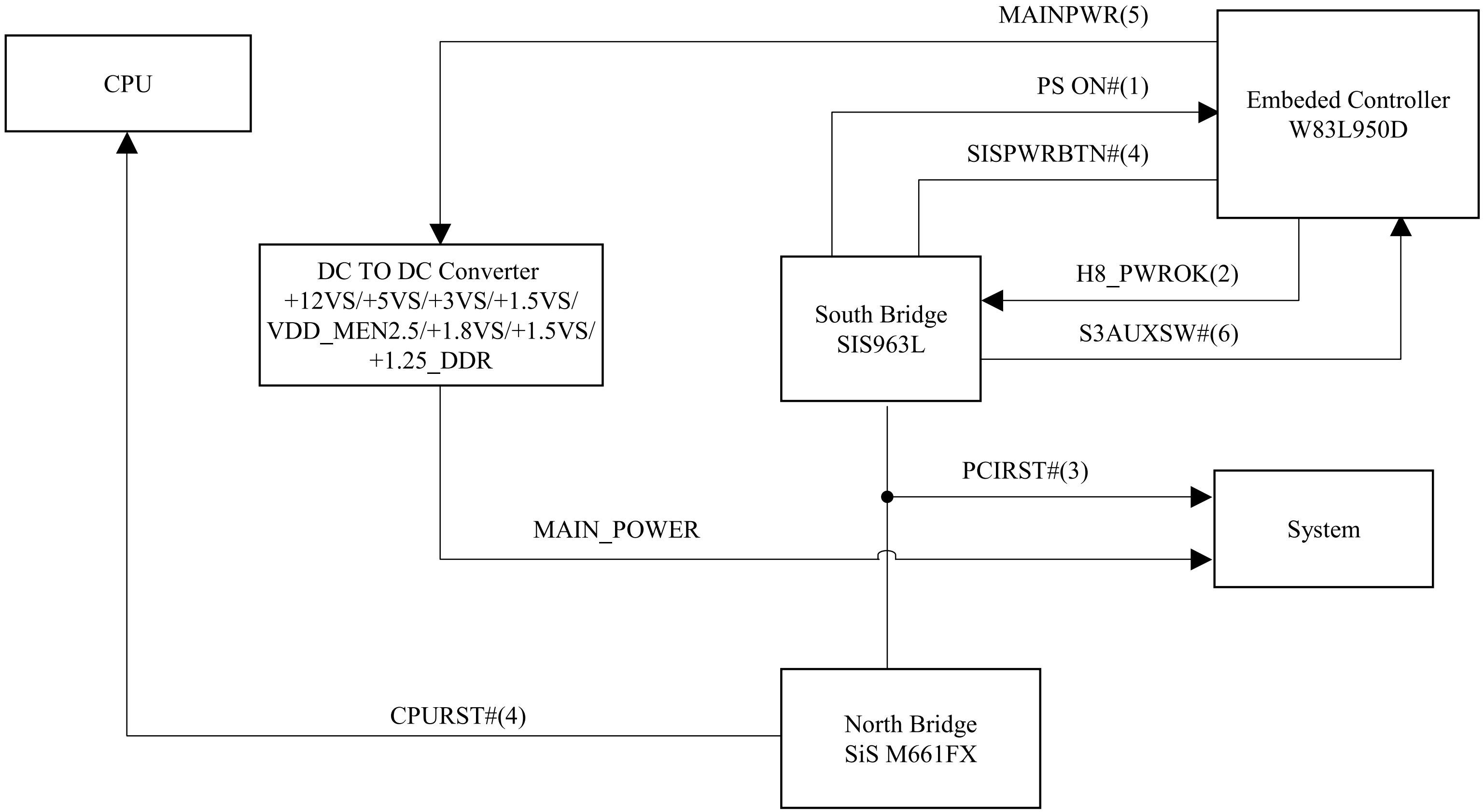
1.3 Electrical Characteristic

1.3.1 Power On Sequence


8599 Power on Sequence Flow Chart
Press Power Button
Power BTN#(1)
Embeded Controller
W83L950D
PWR_ON(2)
DC to DC Converter
+2.5V_DDR/1.8V/+3V/
+5V/+12V/+1.5V
AUXOK(3)
South Bridge
SIS963L
SISPWRBTN#((4)
PS ON#(5)
Main power(6)
DC TO DC Converter
+12VS/+5VS/+3VS/+1.5VS/
VDD_MEN2.5/+1.8VS/+1.5VS/
+1.25_DDR
+5VS
LDO
VCCPVID(7)
CPU
CPU_CORE_EN(8)
DC TO DC Converter
+VCC_CORE
H8_PWROK(9)
Standby_Power
PCIRST#(10)
MAIN_POWER
System
North Bridge
SiS M661FX
CPUPWRGD(11)
CPURST#(12)

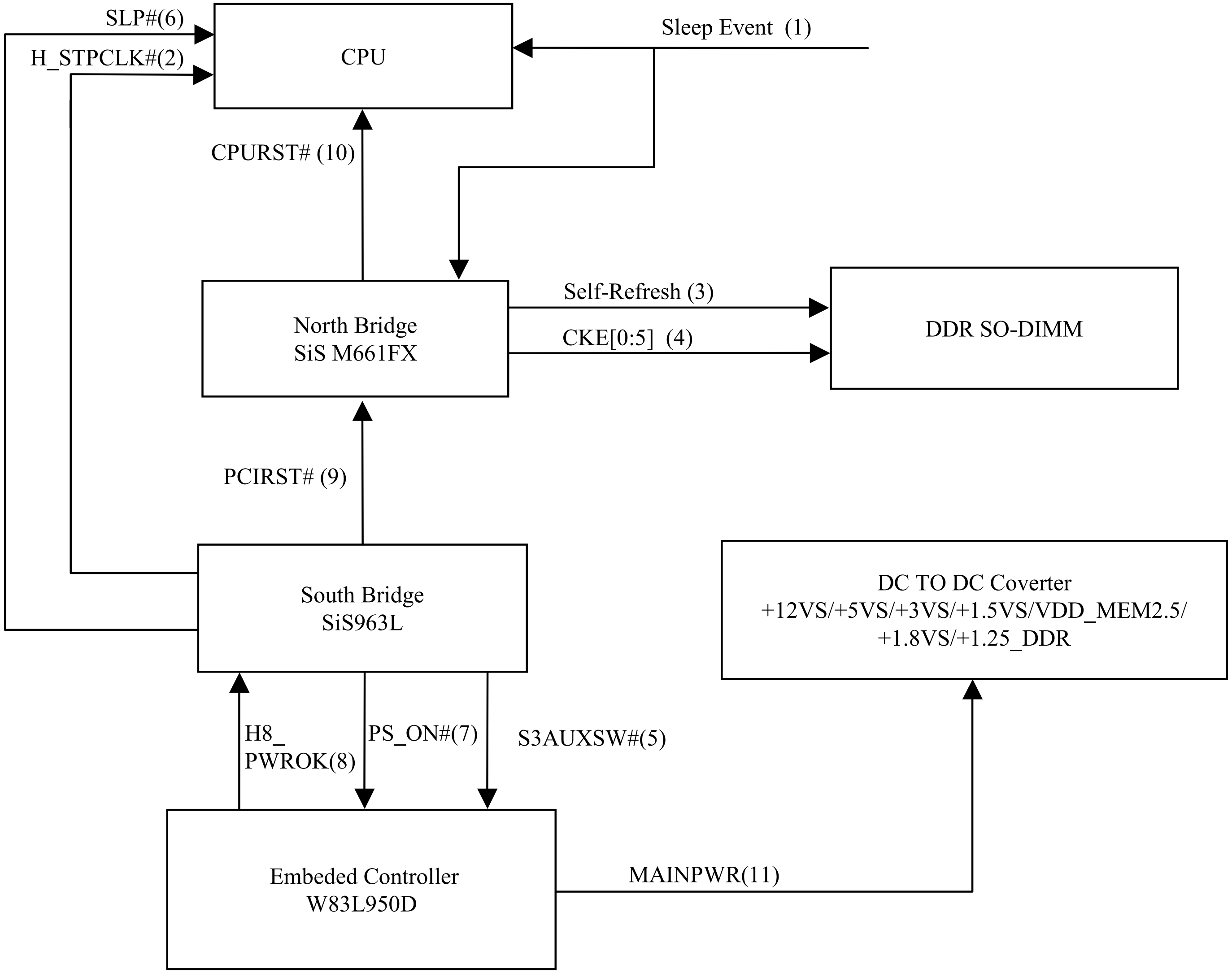
1.3.2 Power Off Sequence

8599 Power off Sequence Flow Chart


MAINPWR(5)
CPU
PS ON#(1)
Embeded Controller
W83L950D
SISPWRBTN#(4)
DC TO DC Converter
+12VS/+5VS/+3VS/+1.5VS/
VDD_MEN2.5/+1.8VS/+1.5VS/
+1.25_DDR
South Bridge
SIS963L
H8_PWROK(2)
S3AUXSW#(6)
PCIRST#(3)
MAIN_POWER
System
CPURST#(4)
North Bridge
SiS M661FX

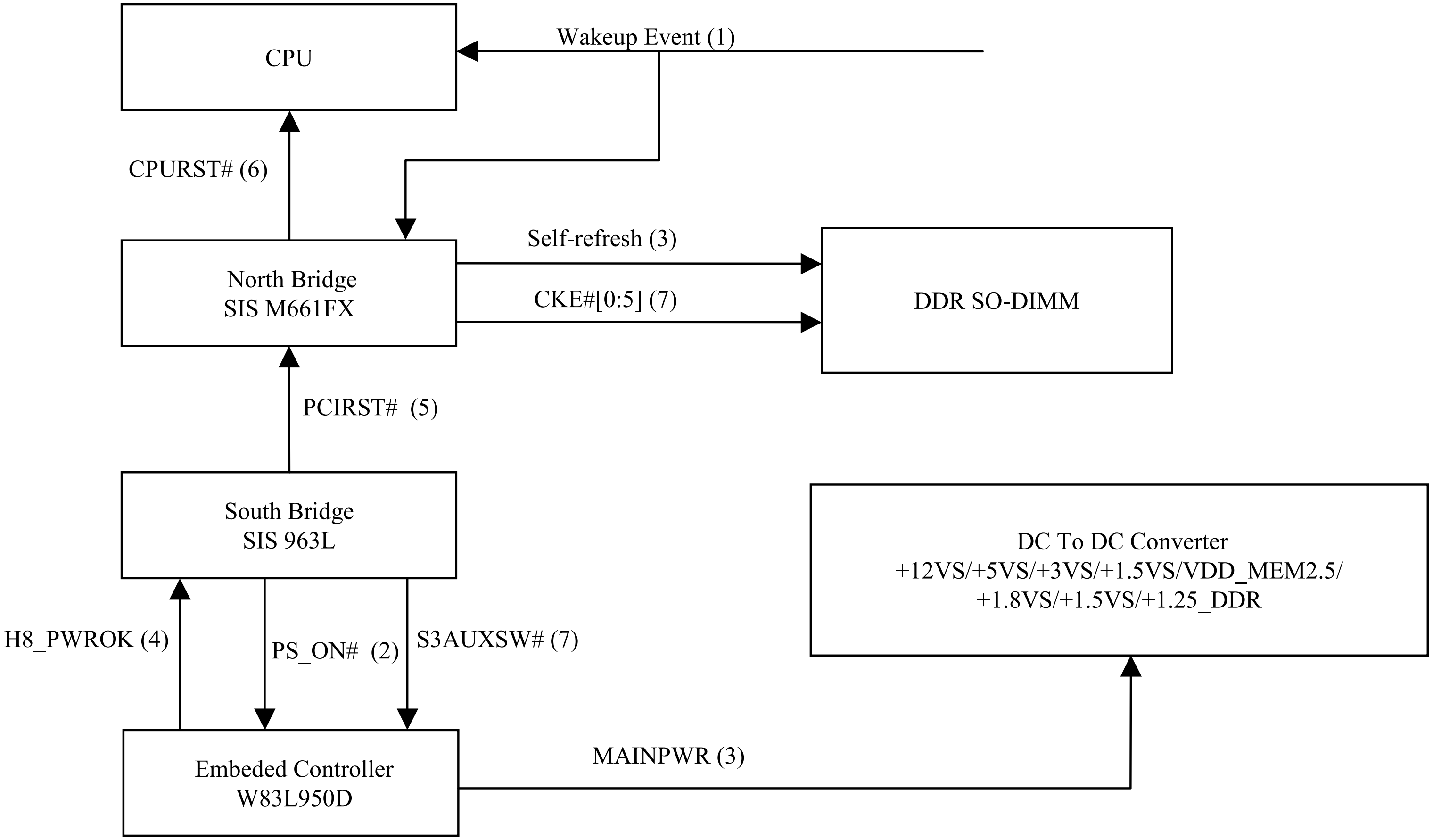
1.3.3 Suspend To RAM Sequence

8599 STR Sequence Flow Chart


SLP#(6)
H_STPCLK#(2)
CPU
Sleep Event (1)
CPURST# (10)
North Bridge
SiS M661FX
Self-Refresh (3)
CKE[0:5] (4)
DDR SO-DIMM
PCIRST# (9)
South Bridge
SiS963L
DC TO DC Coverter
+12VS/+5VS/+3VS/+1.5VS/VDD_MEM2.5/
+1.8VS/+1.25_DDR
H8_
PWROK(8)
PS_ON#(7)
S3AUXSW#(5)
Embeded Controller
W83L950D
MAINPWR(11)

1.3.4 Resume from Suspend To RAM Sequence

8599 Resume From STR Sequence Flow Chart


CPU
Wakeup Event (1)
CPURST# (6)
North Bridge
SIS M661FX
Self-refresh (3)
CKE#[0:5] (7)
DDR SO-DIMM
PCIRST# (5)
South Bridge
SIS 963L
DC To DC Converter
+12VS/+5VS/+3VS/+1.5VS/VDD_MEM2.5/
+1.8VS/+1.5VS/+1.25_DDR
H8_PWROK (4)
PS_ON# (2)
S3AUXSW# (7)
Embeded Controller
W83L950D
MAINPWR (3)

1.3.5 Power Consumption Of Suspend Mode

- Suspend to RAM < 40mA
- Suspend to Disk / Soft-Off /Mechanical Off < 1mA

1.4 Appendix 1: SiS963L GPIO Definitions

Pin Name	Pin Function	Signal Name	Type Define	Power Plan
GPIO0	GPIO	ENBKL_NAME	O	MAIN
GPIO1	GPIO	FLASH	O	MAIN
GPIO2	GPIO	SB_THRM#	I	MAIN
GPIO3	GPIO	EXTSMI#	I	MAIN
GPIO4	GPIO	CLKRUN#	I/O	MAIN
GPIO5	GPIO	MPCI_PD#	I	MAIN
GPIO6	GPIO	SPK_OFF#	O	MAIN
GPIO7	GPIO	GPWAK#	T/P	AUX
GPIO8	GPIO	WAKE_UP#	I	AUX
GPIO9	GPIO	SCI#	I	AUX
GPIO10	GPIO	CRT_IN#	I	AUX
GPIO11	GPIO	STP_PCI#	O	AUX
GPIO12	GPIO	CPU_STP#	O	AUX
GPIO13	GPIO	DPRSLPVR	O	AUX
GPIO14	GPIO	LCD_ID0	I	AUX
GPIO15	GPIO	GMUXSEL	T/P	AUX
GPIO16	GPO	CPUPERF#	O	AUX
GPIO17	GPO	N/A	T/P	AUX
GPIO18	GPO	N/A	T/P	AUX
GPIO19	GPIO	SMBCLK	I/O	AUX
GPIO20	GPIO	SMBDATA	I/O	AUX
GPIO21	GPI	GPIO21_EESK		AUX
GPIO22	GPI	GPIO22_EEDI		AUX
GPIO23	GPI	GPIO23_EEDO		AUX
GPIO24	GPI	GPIO24_EECS		AUX
APICD0			NC	MAIN(GTL LEVEL
APICD1			NC	MAIN(GTL LEVEL
APICCLK			NC	MAIN
OC5	GPI			AUX

1.5 Appendix 2: Keyboard Controller Pin Definitions (1)

Pin	Port	Signal Name	Type	Description
39~54	GP17~GP0	KO[0..15]	O	Keyboard Matrix
55~62	GP37~GP30	KI[7..0]	O	Keyboard Matrix
65~68	GP85~GP82	LAD[0..3]	I/O	LPC BUS
70	GP80	PCI_KBCLK	I	LPC CLK
69	GP81	SERIRQ	O	Serial IRQ
64	GP86	KBCLRST#	I	LPC Reset
63	GP87	LFRAME#	I/O	LPC FRAME
17	GP50	MAINPWR	O	We use this signal to control "VS" power on/off. HI:ON,LOW:OFF
15	GP52	SUSB#	I	STR Indicator signal
14	GP53	ADEN#	I	ADAPTOR IN
23	GP42	SW_+5VA	O	Switch +5VA
22	GP43	COVER_SW#	I	LCD Cover switch
19	GP46	SCI	O	Connect to South Bridge (SiS963L) to system configuration interrupt (ACPI mode)
3	GP76	BAT_DATA	I/O	SMBUS DATA for LM86 themal sensor & BATT THERMAL
2	GP77	BAT_CLK	I/O	SMBUS CLK for LM87 themal sensor & BATT THERMAL
27	GP40	FAN0	O	Control CPU FAN ON & Tum ON/OFF Duty
26	GP41	FAN1	O	Control System D/D FAN (Second FAN) ON & Tum ON/OFF Duty
13	GP54	FAN0_SPD0	I	Return FAN0 (CPU FAN) Speed
12	GP55	FAN0_SPD1	I	Return FAN0 (Second FAN) Speed
16	GP51	BATT_DEAD#	I	Indicated the battery capacity is not enough to power on system
18	GP47	PWRON	O	Control System Power ON/OFF
21	GP44	NUM#	O	Keyboard Number Lock indicator
20	GP45	CAP#	O	Keyboard CAPs Lock indicator
9	GP70	T_DATA	I/O	Conneter to touch Pad DATA
8	GP71	LEARNING#	I	Battery discharge control
7	GP72	SIS_PWRBTN#	O	Power Button Signal to SiS963L
6	GP73	T_CLK	I/O	Connect to Touch Pad clock

1.5 Appendix 2: Keyboard Controller Pin Definitions (2)

Continue to the previous page

Pin	Port	Signal Name	Type	Description
5	GP74	PWROK	O	System Power Good
4	GP75	PSON#_SB	I	System inter S4~S5,Positive Logic
38	GP20	SB_THRM#	O	TO SiS963L,Regustang the sysytem toenter power mangmentmode,Clock Throtting
37	GP21	WAKE_UP#	O	Connect to South Bridge (SiS963L) to wake up system
36	GP22	BATT_G#	O	The indicator when battery in charging
35	GP23	BATT_R#	O	The indicator when battery in charging
34	GP24	EXTSM#	O	Connect to South Bridge (SiS963L) to system management interrupt (Non-ACPI mode)
33	GP25	BATT_POWER#	O	The indicater when power supply from Battery
32	GP26	SCROLL#	O	Keyboard scroll lock indicator
31	GP27	AC_POWER#	O	The indicator when power supply from AC-Adapter
11	GP56	BLADJ	O	Back/Light Adijust Control
10	GP57	CHG_I	O	Supply current to Battery
1	GP60	PWRBTN#	I	Power Switch Signal to KBC
80	GP61	VRMPWRGD	I	CPU Power Good
79	GP62	+3V	I	
78	GP63	BAT_TEMP	I	Report Battery Thermal
77	GP64	BAT_VOLT	I	Report Battery Voltage
76	GP65	I_LIMIT	I	FOR BATTERY CHARGE I limit
75	GP66	I_CHG	I	Battery charge current
74	GP67	I_DISCHG	I	Battery discharge current
25	RESET#	RESET#	I	KBC Reset
28	XIN	XIN		
29	XOUT	XOUT		
72	VREF	+3VA		
71	VCC	+KBC_VDDA		

1.6 Appendix 3: Audio Performance

8599 meet all the following items

Table 9. Digital Playback (PC-D-A) for Line Output

Test Items	Mobile System
Full Scale Output Voltage	≧0.7Vrms (3.3V audio)
Sample Frequency Accuracy	≦0.1%
Frequency Response (44.1ks/sec)	20Hz～15kHz
Frequency Response (48ks/sec)	20Hz～15kHz
Dynamic Range (SNR)	≧70dBFSA
THD+N	≦-55dBFS
Cross-talk	≧50dB

Table 10. Analog Pass-through(A-A) for Microphone Input to Line Output

Test Items	Mobile System
Frequency Response	100Hz～12kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

Table 11. Digital Recording(A-D-PC) for Microphone Input

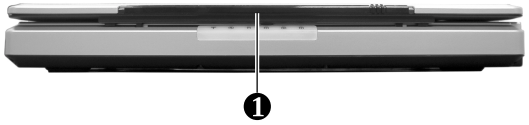
Test Items	Mobile System
Full Scale Input Voltage	≧100mVrms
Sample Frequency Accuracy	≦0.1%
Frequency Response(22.05ks/sec)	100Hz～8.8kHz
Dynamic Range (SNR)	≧60dBFSA
THD+N	≦-50dBFS

2. System View and Disassembly

2.1 System View

2.1.1 Front View

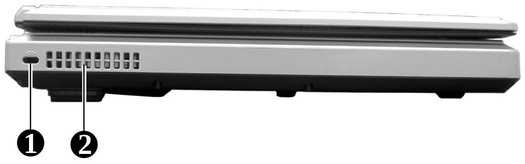
❶ Top Cover Latch



2.1.2 Left-side View

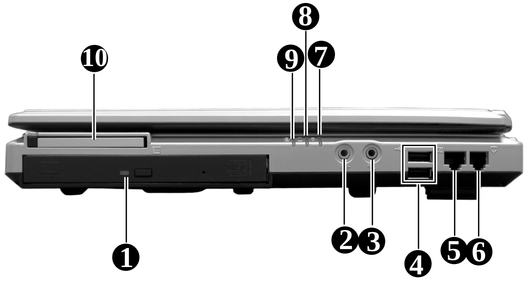
❶ Lock

❷ Ventilation Openings



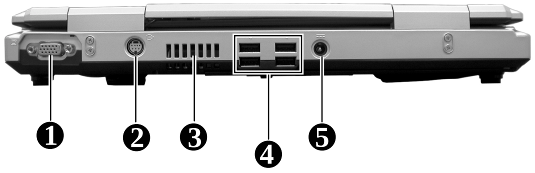
2.1.3 Right-side View

❶ CD/DVD driver
❷ Line out jack
❸ MIC in jack
❹ USB port *2
❺ RJ-45 connector
❻ RJ-11 connector
❼ AC Power Indicator
❽ Battery Power Indicator
❾ Battery Charge Indicator
❿ PC Card slot



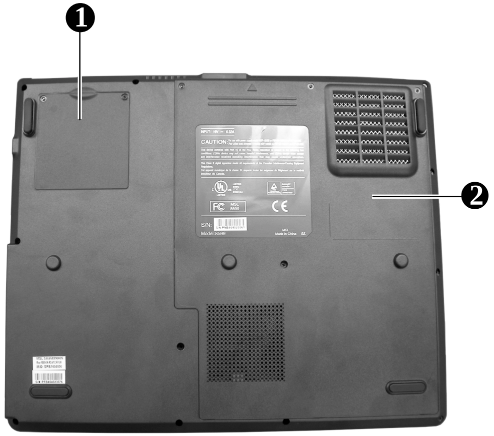
2.1.4 Rear View

❶ VGA port
❷ S-Video output connector
❸ Ventilation Openings
❹ USB port *4
❺ Power connector



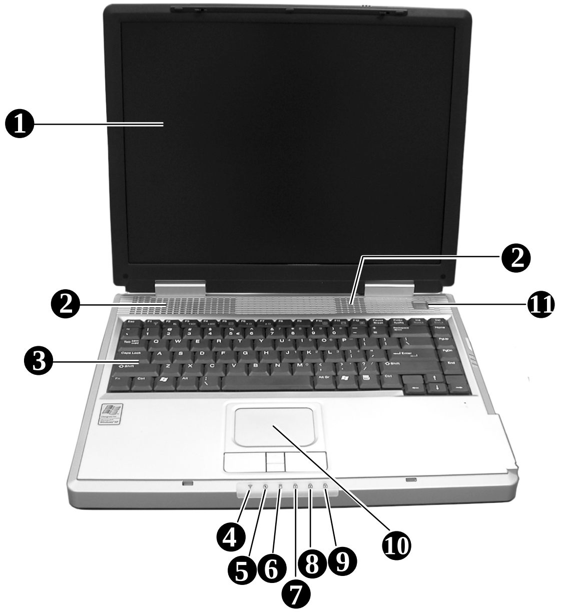
2.1.5 Bottom View

- ❶ Wireless Card cover
- ❷ CPU



2.1.6 Top-open View

- ❶ LCD Screen
- ❷ Stereo set
- ❸ Keyboard
- ❹ Caps Lock
- ❺ Wireless Card Indicator
- ❻ CD/DVD-Rom Indicator
- ❼ HDD Indicator
- ❽ Num Lock
- ❾ Caps Lock
- ❿ Scroll Lock
- ⓫ Power Button



2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations. Use the chart below to determine the disassembly sequence for removing components from the notebook.

NOTE: *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*

- **NOTEBOOK**
  - **Modular Components**
    - **2.2.1 Battery Pack**
    - **2.2.2 Keyboard**
    - **2.2.3 CPU**
    - **2.2.4 HDD Module**
    - **2.2.5 DVD-ROM Drive**
    - **2.2.6 DIMM module**
    - **2.2.7 Modem Card**
  - **LCD Assembly Components**
    - **2.2.7 LCD Assembly**
    - **2.2.8 Inverter Board**
    - **2.2.9 LCD Panel**
  - **Base Unit Components**
    - **2.2.10 System Board**
    - **2.2.11 Touch Pad**

2.2.1 Battery Pack

Disassembly

1. Carefully put the notebook upside down.
2. Remove the four screws, then remove the CPU cover. (Figure 2-1)
3. Put up the battery pack, then free the battery pack. (Figure 2-2)

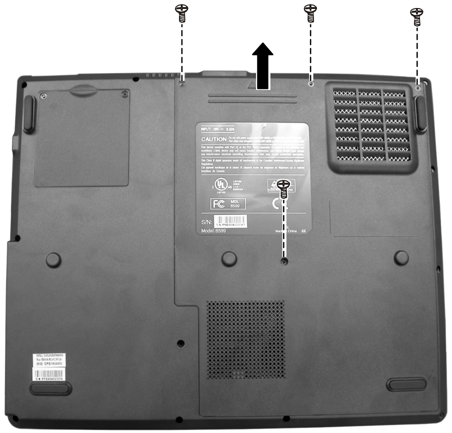


Figure 2-1 Remove the four screws

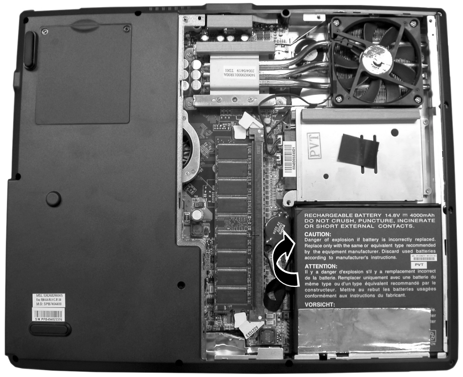


Figure 2-2 Remove the battery pack

Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Replace the CPU cover and secure the four screws.

2.2.2 Keyboard

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Open the top cover.
3. Loosen the five latches locking the keyboard. (Figure 2-3)

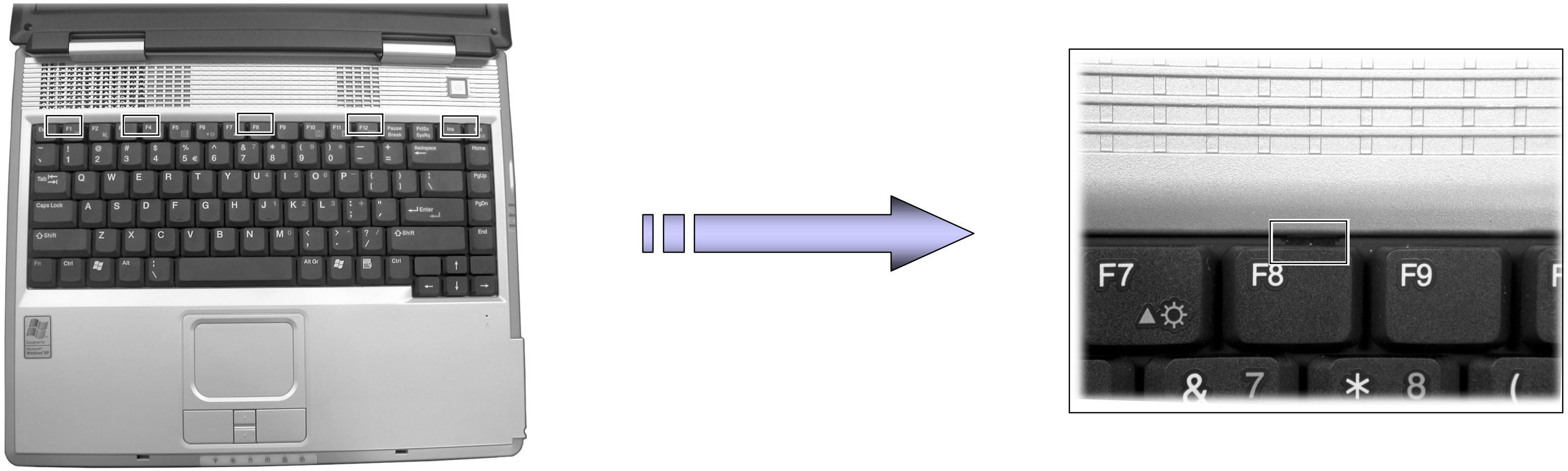


Figure 2-3 Loosen the five latches

4. Slightly lift up the keyboard and disconnect the cable from the mother board, then separate the keyboard. (Figure 2-4)

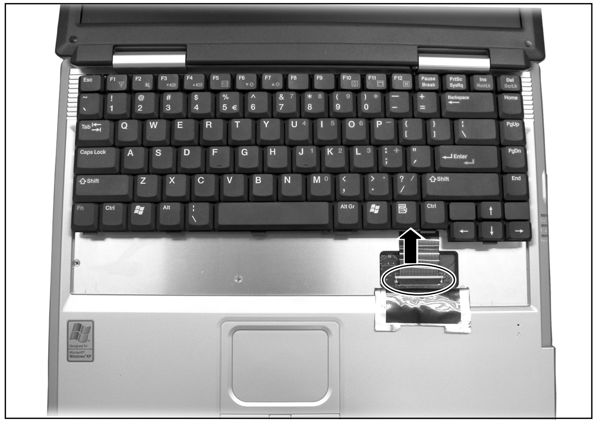


Figure 2-4 Lift up the keyboard and disconnect the cable

Reassembly

1. Reconnect the keyboard cable and fit the keyboard back.
2. Replace the keyboard into place and fasten the five latches.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.3 CPU

Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove five screws that secure the heatsink upon the CPU. (Figure 2-5)
3. Disconnect the fan's power cord from system board. (Figure 2-6)

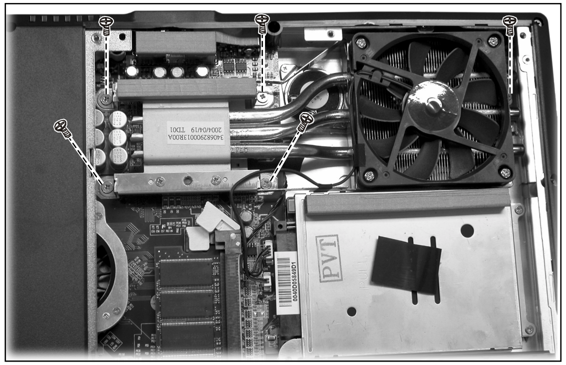


Figure 2-5 Remove five screws

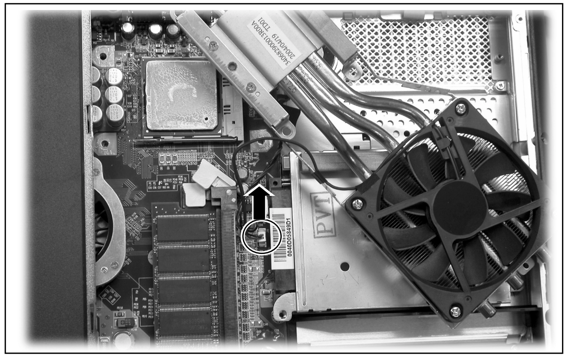


Figure 2-6 Disconnect the cable

4. To remove the existing CPU, lift the socket arm up to the vertical position. (Figure 2-7)

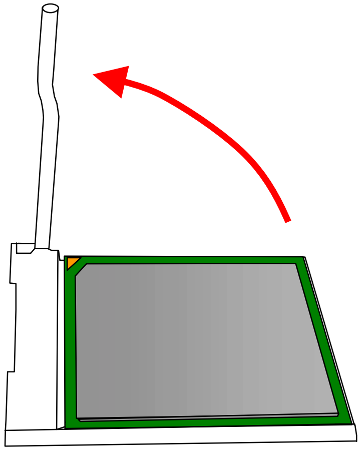


Figure 2-7 Free the CPU

Reassembly

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Place the lever back to the horizontal position and push the lever to the left.
2. Reconnect the fan's power cord to the system board, fit the heatsink onto the top of the CPU and secure with five screws.
3. Replace the battery pack. (See section 2.2.1 reassembly)

2.2.4 HDD Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the HDD module and slightly lift up HDD module. (Figure 2-8)
3. Remove four screws to separate the hard disk drive from the bracket, free the hard disk driver. (Figure 2-9)

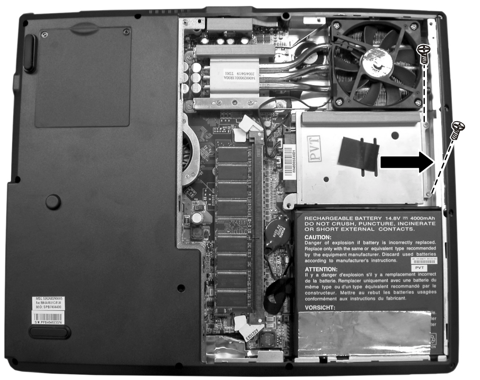


Figure 2-8 Remove HDD module

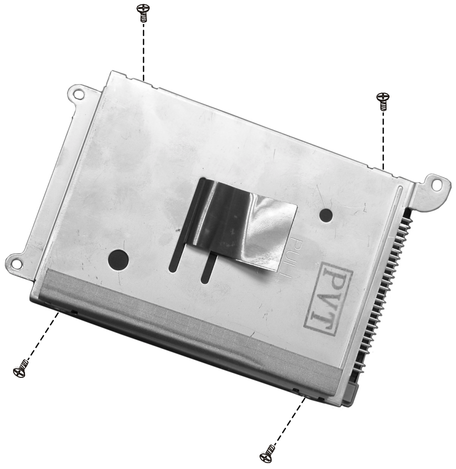


Figure 2-9 Free the HDD driver

Reassembly

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with two screws.
3. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.5 CD/DVD-ROM Drive

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove two screws fastening the CD/DVD-ROM drive. (Figure 2-10)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out(❷). (Figure 2-10)

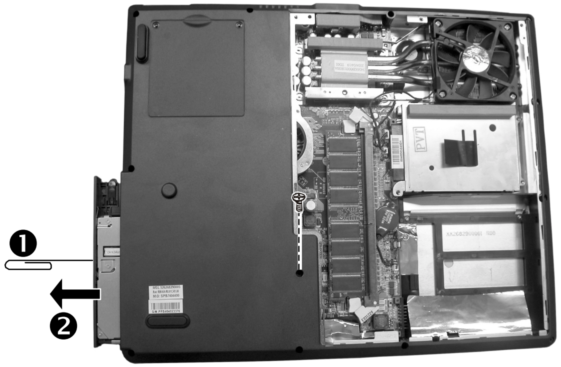


Figure 2-10 Remove the CD/DVD-ROM drive

Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.6 DIMM Module

Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. To remove the memory module, pull the retaining clips outwards to the unlocked and lift the DIMM module up. (Figure 2-11)

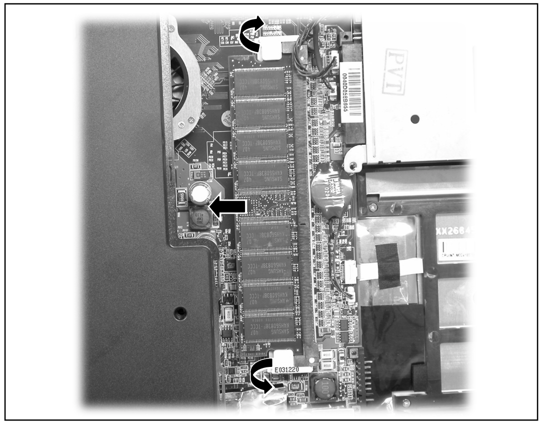


Figure 2-11 Remove the DIMM module

Reassembly

1. Replace DIMM module and lock it retaining clips.
2. Replace the battery pack. (Refer to section 2.2.1 reassembly)

2.2.7 Modem Card

Disassembly

1. Remove the battery, keyboard, CPU, hard disk driver, CD/DVD-ROM driver. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5 Disassembly)
2. Remove the four screws. (Figure 2-12)
3. Remove the eleven screws and put up the housing. (Figure 2-13)

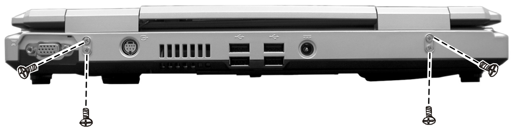


Figure 2-12 Remove eleven screws

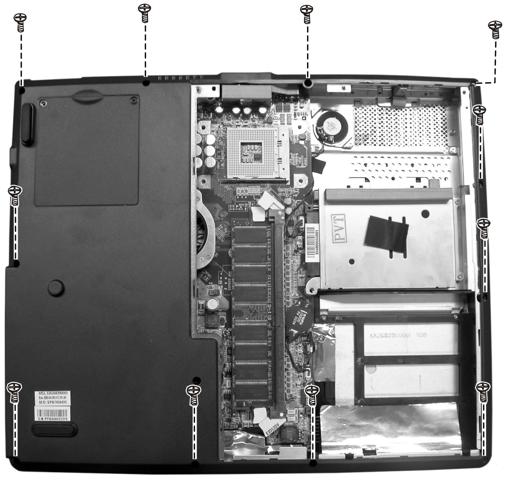


Figure 2-13 Free the housing

8599 N/B Maintenance

4. Remove three screws and free the bottom shielding. (Figure 2-14)
5. Disconnect the cable and remove the two screws. (Figure 2-15)

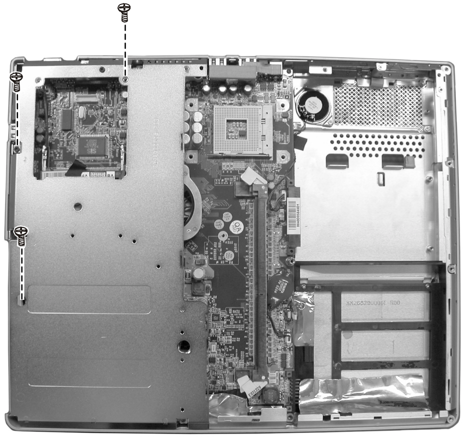


Figure 2-14 Free the bottom shielding

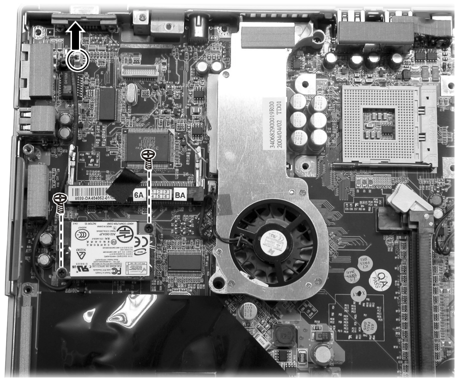


Figure 2-15 Free the Modem Card

Reassembly

1. Replace the modem card and secure two screws.
2. Reconnect the cable to the system board.
3. Replace the bottom shielding and secure the three screws.
4. Fit the top cover and the housing, then secure the fifteen screws.
5. Replace CD/DVD-ROM, HDD, CPU, keyboard and battery pack. (See sections 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.8 LCD ASSY

Disassembly

1. Remove the battery pack and keyboard. (See sections 2.2.1 and 2.2.2 Disassembly)
2. Remove two hinge covers. (Figure 2-16)
3. Carefully put the notebook upside down. Remove the two screws fastening the wireless cover. (Figure 2-17)

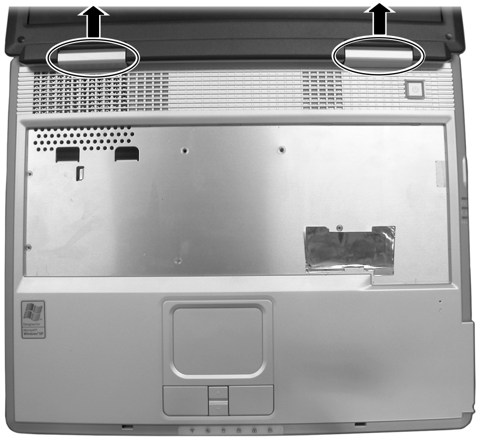


Figure 2-16 Remove two hinge covers

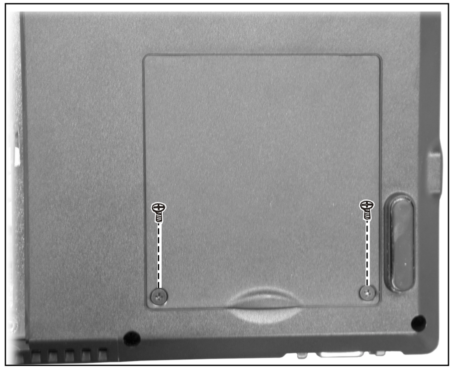


Figure 2-17 Remove the two screws

4. Disconnect the LCD cable from the system board and detach the antenna. (Figure 2-18)
5. Remove the four screws and put up the LCD assembly, then free the LCD assembly. (Figure 2-19)

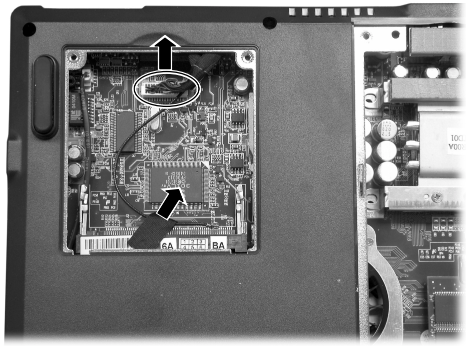


Figure 2-18 Disconnect the LCD cable

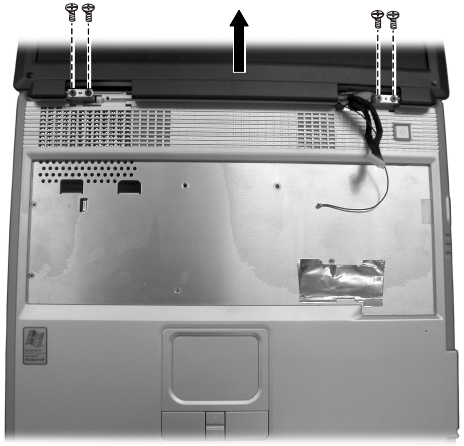


Figure 2-19 Free the LCD assembly

Reassembly

1. Attach the LCD assembly to the base unit and secure with four screws, then fit the antenna.
2. Reconnect the one cable to the system board, Then replace the wireless cover and secure two screws.
3. Replace the two hinge covers.
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.9 Inverter Board

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to section 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove two screws and rubbers on the corners of the LCD panel. (Figure 2-20)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the one screw fastening the inverter board. (Figure 2-21)

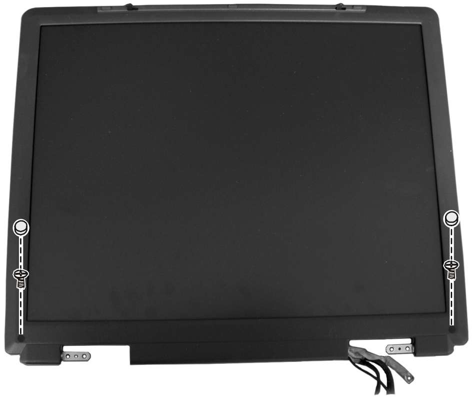


Figure 2-20 Remove LCD cover

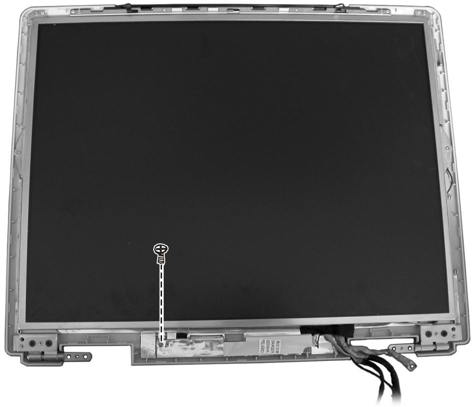


Figure 2-21 Remove the one screw

5. To remove the inverter board on the lower part of the LCD housing , disconnect two cables. (Figure 2-22)

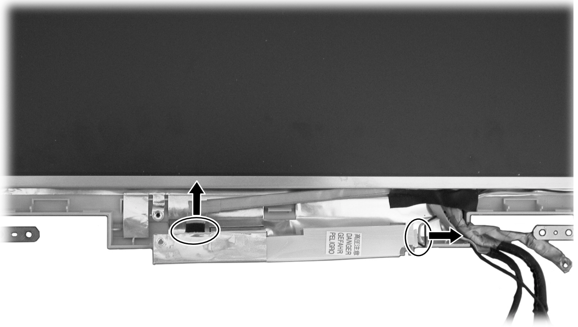


Figure 2-22 Remove the inverter board

Reassembly

1. Reconnect the two cables. Fit the inverter board back into place and secure with one screw.
2. Replace the LCD cover and secure with two screws and rubbers.
3. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
4. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.10 LCD Panel

Disassembly

1. Remove the battery, keyboard and LCD assembly. (Refer to sections 2.2.1, 2.2.2 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer for two steps 2,3 of section 2.2.9 Disassembly)
3. Remove the eight screws fastening the LCD panel and detach the cable, Then lift it up. (Figure 2-23)
4. Remove the five screws fastening the LCD brackets. (Figure 2-24)

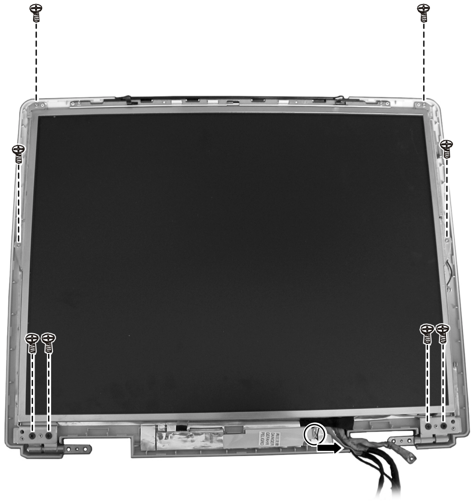


Figure 2-23 Remove the eight screws and detach the cable

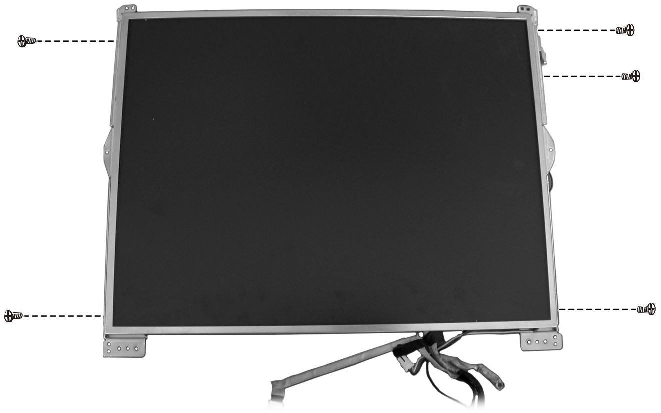


Figure 2-24 Remove the five screws

5. Disconnect the cable and free the LCD panel. (Figure 2-25)

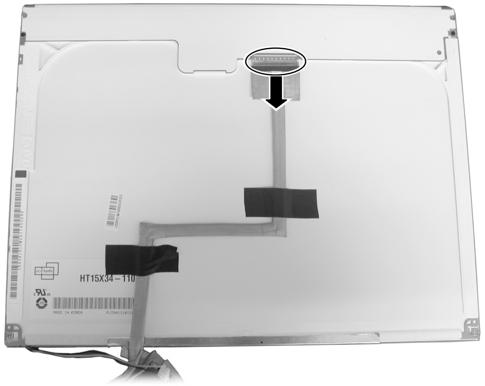


Figure 2-25 Free the LCD panel

Reassembly

1. Reconnect the cable, then replace the LCD brackets and secure with five screws.
2. Fit the LCD panel back into place and secure with eight screws, then reconnect the cable to the inverter board.
3. Replace the LCD cover and secure with two screws and rubbers. (Refer to section 2.2.9 Reassembly)
4. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
5. Replace the keyboard and battery pack. (Refer to sections 2.2.2 and 2.2.1 Reassembly)

2.2.11 System Board

Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, DIMM module, modem card and LCD assembly. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Disconnect the heatsink's cable from the system board and remove two screws fastening the heatsink. (Figure 2-26)
3. Disconnect the speaker's cable and the touch pad's cable from the system board.To free the system board, please remove one screw and four hex nuts that fastening the system board. (Figure 2-27)

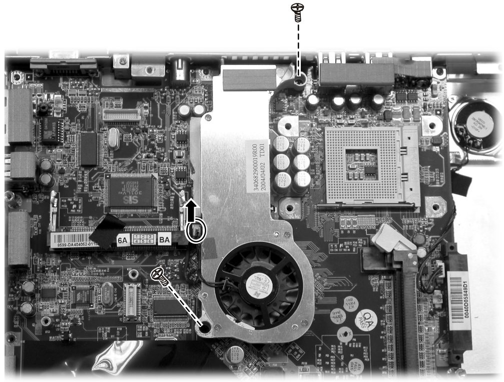


Figure 2-26 Free the heatsink

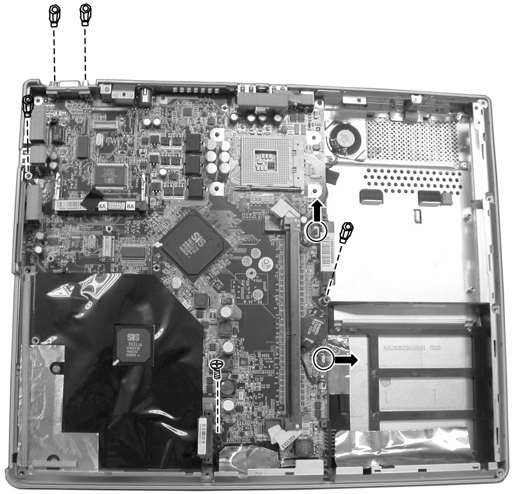


Figure 2-27 Free the system board

Reassembly

1. Replace the system board into the top cover and secure with one screw and four hex nuts.
2. Reconnect the touch pad's cable, the speaker's cable.
3. Replace the heatsink and secure the two screws, then reconnect the cable to the system board.
4. Replace the modem card. (See sections 2.2.7 reassembly)
5. Replace the LCD assembly, DIMM module, CD/DVD-ROM, HDD, CPU, keyboard and battery pack. (See sections 2.2.8, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

2.2.12 Touch Pad

Disassembly

1. Remove the system board. (See section 2.2.11 Disassembly)
2. Remove the two screws and disconnect the cable, then free the touch pad. (Figure 2-28)

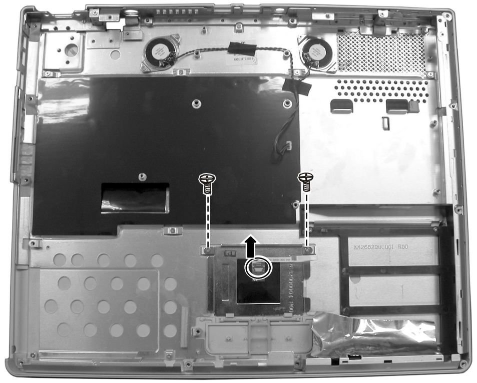


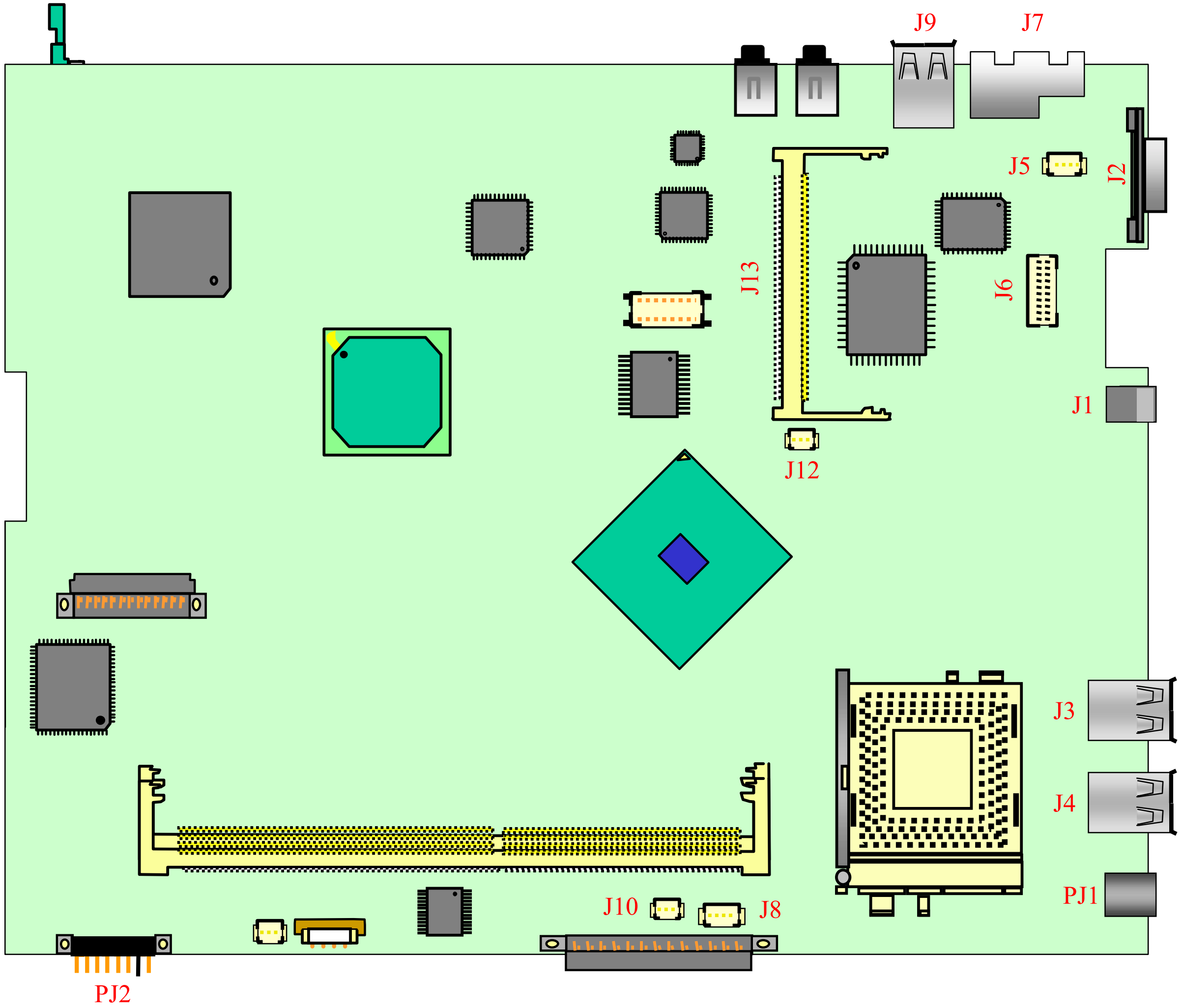
Figure 2-28 Free the touch pad

Reassembly

1. Replace the touch pad and reconnect the cable.
2. Replace the touch pad shielding and secure with two screws.
3. Reassemble the notebook. (See the previous sections Reassembly)

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 1

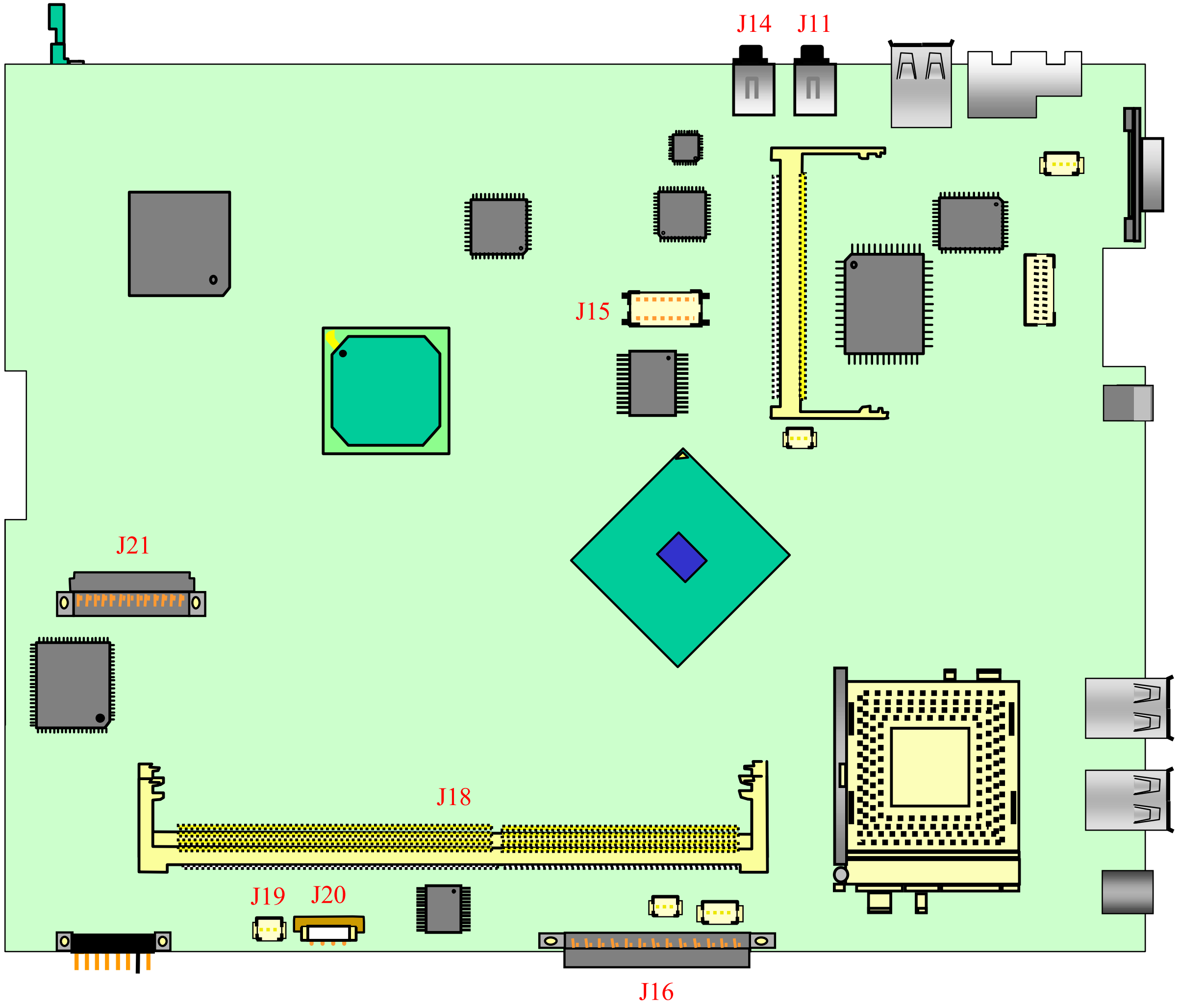


- **PJ1 : AC Power Jack**
- **PJ2 : Battery Connector**
- **J1 : S-Video Port**
- **J2 : External VGA Connector**
- **J3, J4, J9 : USB Port Connector**
- **J5 : MDC Jump Wire Connector**
- **J6 : LCD Connector + Inverter**
- **J7 : RJ11 & RJ45 Connector**
- **J8 : Internal Left Speak Connector**
- **J10 : CPU Fan Connector**
- **J12 : NB Fan Connector**
- **J13 : Mini-PCI Socket**

------ To next page ------

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side A) - 2



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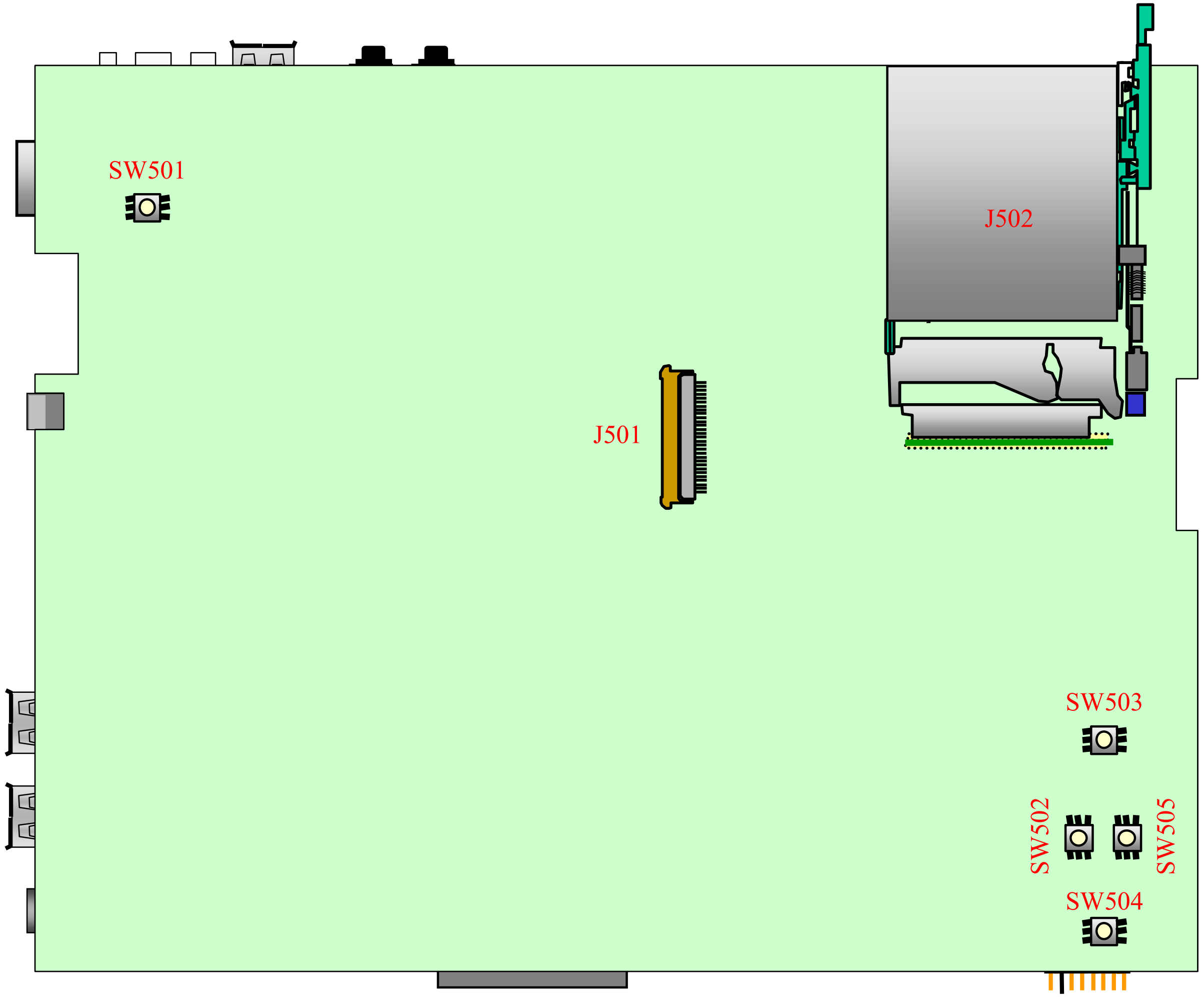
- **J11 : MIC In Jack**
- **J14 : Line Out Jack**
- **J15 : MDC Board Connector**
- **J16 : Primary EIDE Connector**
- **J18 : Extend DDR SDRAM Socket**
- **J19 : RTC Battery Connector**
- **J20 : Touch-Pad Connector**
- **J21 : Secondary IDE Connector**

3. Definition & Location of Connectors / Switches

3.1 Mother Board (Side B)

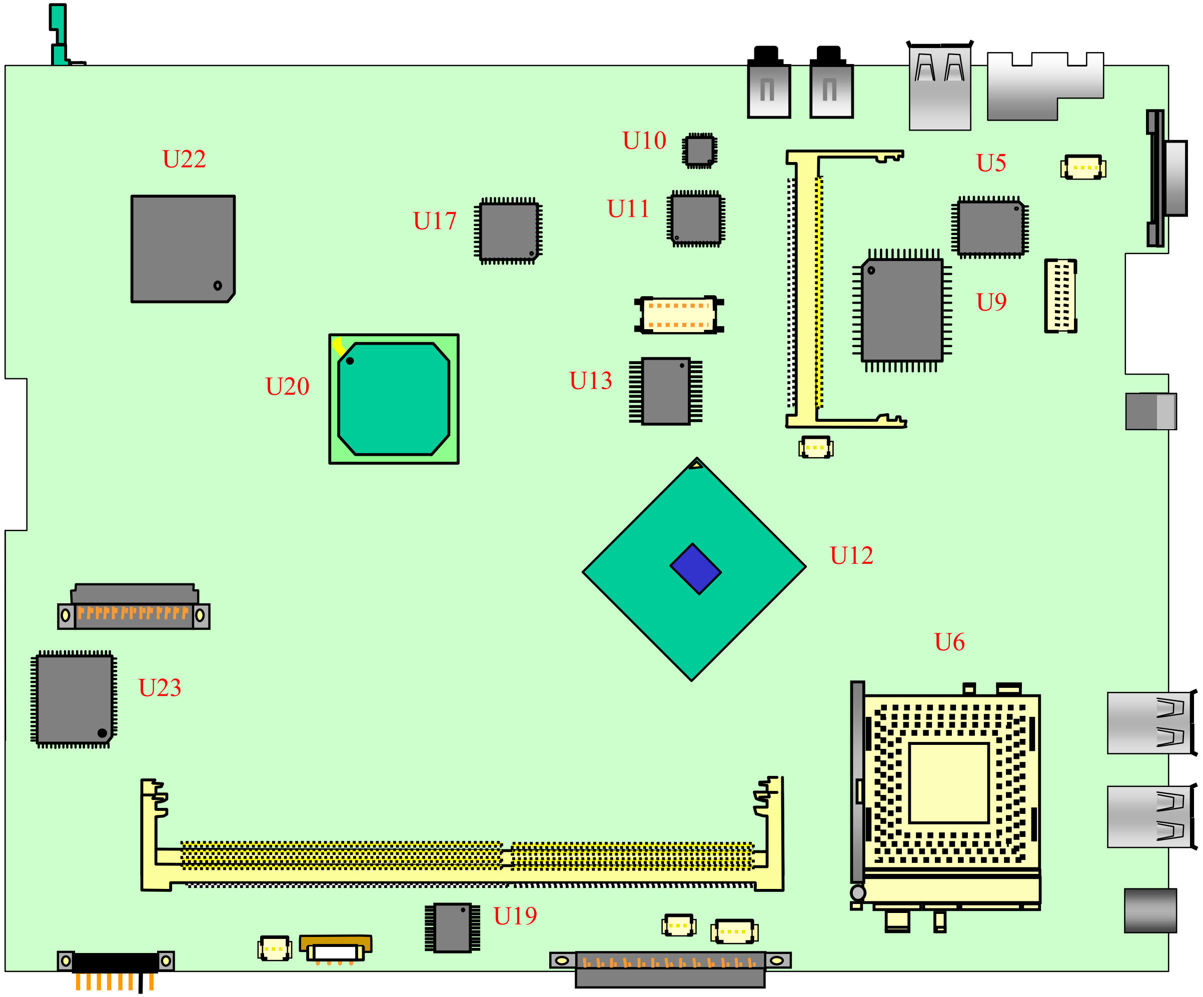

SW501
J502
J501
SW503
SW502
SW505
SW504

- **J501 : Internal Keyboard Connector**
- **J502 : PCMCIA Card Socket**

- **SW501 : Power Button**
- **SW502 : Touch-Pad Up Button**
- **SW503 : Touch-Pad Right Button**
- **SW504 : Touch-Pad Left Button**
- **SW505 : Touch-Pad Down Button**

4. Definition & Location of Major Components

4.1 Mother Board (Side A)



- **U5 : ICS1883AF LAN Controller**
- **U6 : Intel P4 Process Socket**
- **U9 : TV/ LVDS Encoder (SiS301LV)**
- **U10 : GMT G1422 Amplifer**
- **U11 : VIA VI1616 Audio Codec**
- **U12 : SiS M661FX NB**
- **U13 : ICS952007 Clock Generator**
- **U17 : KBC (W83L950D)**
- **U19 : DDR Buffer Clock**
- **U20 : SiS963L SB**
- **U22 : Ti PCI1410A CardBus**
- **U23 : LPC BIOS ROM**

5. Pin Descriptions of Major Components

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 1

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>AP[1:0]#</td><td>Input/
Output</td><td>AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#,A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This allows parity to be high when all the covered signals are high. AP[1:0]# should connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus agents. The following table defines
<table>
<tr><th>Request Signals</th><th>subphase 1</th><th>subphase 2</th></tr>
<tr><td>A[35:24]#</td><td>AP0#</td><td>AP1#</td></tr>
<tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr>
<tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr>
</table></td></tr>
<tr><td>BCLK[1:0]</td><td>Input</td><td>The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs.
All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS} .</td></tr>
<tr><td>BINIT#</td><td>Input/
Output</td><td>BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation.
If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries.
If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</td></tr>
<tr><td>BNR#</td><td>Input/
Output</td><td>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</td></tr>
</table>

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A[35:3]#</td><td>Input/
Output</td><td>A[35:3]# (Address) define a 2^{36} -byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Pentium 4 processor in the 478-pin package system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.</td></tr>
<tr><td>A20M#</td><td>Input</td><td>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode.
A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.</td></tr>
<tr><td>ADS#</td><td>Input/
Output</td><td>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.</td></tr>
<tr><td>ADSTB[1:0]#</td><td>Input/
Output</td><td>Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB0#</td></tr>
<tr><td>A[35:17]#</td><td>ADSTB1#</td></tr>
</table></td></tr>
</table>

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 2

Name	Type	Description
HIT# **HITM#**	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signals does not have on-die termination. Refer to Section 2.5 fortermination requirements.**
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error.IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	The ITPCLKOUT[1:0] pins do not provide any output for the Pentium® 4 processor in the 478-pin package. Refer to Section 2.5 for additional details and termination requirements.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus isreleased after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Pentium 4 processor in the 478-pin package system bus gents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/ Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr>
<tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr>
<tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr>
<tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr>
</table></td></tr>
<tr><td>FERR#</td><td>Output</td><td>FERR# (Floating-point Error) is asserted when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*-type floating-point error reporting.</td></tr>
<tr><td>GTLREF</td><td>Input</td><td>GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the <i>Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide</i> for more information.</td></tr>
</table>

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 3

Name	Type	Description
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. ‘Clean’ implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 11 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 16, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after VCC and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer’s Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 4

Name	Type	Description
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for a details on parity checking of these signals.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also knownas the Test Access Port).

Name	Type	Description
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] **TESTHI[5:0]**	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a VCC power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C.Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (VCC) must be removed following the assertion of THERMTRIP#. See Figure 12 and Table 16 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP# , if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted after RESET# is de-asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.1 Intel Pentium 4 Processor mFC-PGA 478 Pins - 5

Name	Type	Description
VCCIOPLL	Input	VCCIOPLL provides isolated power for internal processor system bus PLLs. Follow he guidelines for VCCA, and refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.
VCCSENSE	Output	VCCSENSE is an isolated low impedance connection to processor core power(VCC). It can be used to sense or measure power near the silicon with little noise.
VCCVID	Input	There is no imput voltage requirement for VCCVID for designs intended tosupport only the Pentium 4 processor in the 478-pin package. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for more information.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins can be used to support automatic selection of power supply voltages (Vcc). These pins are not signals, but are either an open circuit or a short circuit to VSS on the processor. The combination of opens and shorts defines the voltage required by the processor. The VID pins are needed to cleanly support processor voltage specification variations. See Table 2 for definitions of these pins. The power supply must supply the voltage that is requested by these pins, or disable itself.
VSSA	Input	VSSA is the isolated ground for internal PLLs.
VSSSENSE	Output	VSSSENSE is an isolated low impedance connection to processor core VSS. It can be used to sense or measure ground near the silicon with little noise
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 . pull-down resistor.
VCCA	Input	VCCA provides isolated power for the internal processor core PLLs. Refer to the *Intel® Pentium® 4 Processor in the 478-pin Package and Intel® 850 Chipset Platform Design Guide* for complete implementation details.

5.2 SiS M661FX (IGUI Host Memory Controller) - 1

Host Bus Interface

Ball Name	Ball Attr	Description
CPUCLK CPUCLK#	I 0.71V – M	Host differential clock input.
CPURST#	O 0.9~1.8V – M	Host Bus Reset: CPURST# is used to keep all the bus agents in the same initial state before valid cycles issued.
CPUPWRGD	O 0.9~1.8V – M	CPUPWRGD is used to inform CPU that main power is stable
ADS#	I/O 0.9~1.8V – M	Address Strobe : Address Strobe is driven by CPU or SiSM661FX to indicate the start of a CPU bus cycle.
HASTB[1:0]#	I/O 0.9~1.8V – M	Source synchronous address strobe used to latch HREQ[4:0]# & HA[31:3]# at both falling and rising edge. HREQ[4:0]# & HA[16:3]# are latched by HASTB0# HA[31:17]# are latched by HASTB1#
HREQ[4:0]#	I/O 0.9~1.8V – M	Request Command: HREQ[4:0]# are used to define each transaction type during the clock when ADS# is asserted and the clock after ADS# is asserted.
HA[31:3]#	I/O 0.9~1.8V – M	Host Address Bus
BREQ0#	O 0.9~1.8V – M	Symmetric Agent Bus Request: BREQ0# is driven by the symmetric agent to request for the bus.
BPRI#	O 0.9~1.8V – M	Priority Agent Bus Request: BPRI# is driven by the priority agent that wants to request the bus. BPRI# has higher priority than BREQ0# to access a bus.
BNR#	I/O 0.9~1.8V – M	Block Next Request: This signal can be driven asserted by any bus agent to block further requests being pipelined.
HLOCK#	I 0.9~1.8V – M	Host Lock : CPU asserts HLOCK# to indicate the current bus cycle is locked.
HIT#	I/O 0.9~1.8V – M	Keeping a Non-Modified Cache Line

Host Bus Interface (Continued)

Ball Name	Ball Attr	Description
HITM#	I/O 0.9~1.8V – M	Hits a Modified Cache Line: Hit Modified indicates the snoop cycle hits a modified line in the L1/L2 cache of CPU.
DEFER#	O 0.9~1.8V – M	Defer Transaction Completion: SiSM661FX will use this signal to indicate a retry or defer response to host bus.
RS[2:0]#	O 0.9~1.8V – M	Response Status: RS[2:0]# are driven by the response agent to indicate the transaction response type. The following shows the response type. RS[2:0]# Response 000 Idle State 001 Retry 010 Defer 011 Reserved 100 Reserved 101 No data 110 Implicit Write-back 111 Normal
HTRDY#	O 0.9~1.8V – M	Target Ready: During write cycles, response agent will drive TRDY# to indicate it is ready to accept data.
DRDY#	I/O 0.9~1.8V – M	Data Ready: DRDY# is driven by the bus owner whenever the data is valid on the bus.
DBSY#	I/O 0.9~1.8V – M	Data Bus Busy: Whenever the data is not valid on the bus with DRDY# is deserted, DBSY# deasserted to hold the bus.
HD[63:0]#	I/O 0.9~1.8V – M	Host Data Bus
DBI[3:0]#	I/O 0.9~1.8V – M	Dynamic Bus Inversion: An active DBI# will invert it’s corresponding data group signals. DBI0# is referenced by HD[15:0]# DBI1# is referenced by HD[31:16]# DBI2# is referenced by HD[47:32]# DBI3# is referenced by HD[63:48]#

5.2 SiS M661FX (IGUI Host Memory Controller) - 2

Host Bus Interface (Continued)

Ball Name	Ball Attr	Description
HDSTBP[3:0]#	I/O 0.9~1.8V – M	Source synchronous data strobe used to latch data at falling edge HD[15:0]#, DBI0# are latched by HDSTBP0# HD[31:16]#, DBI1# are latched by HDSTBP1# HD[47:32]#, DBI2# are latched by HDSTBP2# HD[63:48]#, DBI3# are latched by HDSTBP3#
HDSTBN[3:0]#	I/O 0.9~1.8V– M	Source synchronous data strobe used to latch data at falling edge HD[15:0]#, DBI0# are latched by HDSTBN0# HD[31:16]#, DBI1# are latched by HDSTBN1# HD[47:32]#, DBI2# are latched by HDSTBN2# HD[63:48]#, DBI3# are latched by HDSTBN3#
HCOMP_N	I M	GTL N-MOS Compensation Input
HCOMP_P	I M	GTL P- MOS Compensation Input
HVREF[4:0] HCOMPVREF_N	I M	AGTL+ I/O reference voltage

MuTIOL® 1G Interface

Pin Name	Pin Attr	Description
ZCLK	I 3.3V - M	SiS MuTIOL ? ?G clock
ZUREQ/ZDREQ	I/O 1.8V - M	SiS MuTIOL ? ?G Control pins
ZSTB[1:0]	I/O 1.8V - M	SiS MuTIOL ? ?G Strobe
ZSTB[1:0]#	I/O 1.8V - M	Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	Address/Data/DBI Pins
ZVREF	I M	SiS MuTIOL ? ?G Reference Voltage
ZCMP_N	I M	N-MOS Compensation Input
ZCMP_P	I M	P-MOS Compensation Input

DRAM Controller

Ball Name	Ball Attr	Description
DRAMTEST	I 2.5V - M	Test Clock Input
FWDSDCLKO	O 2.5V – M	SDRAM Forward Clock Output
MA[14:0]	O 2.5V - M	System Memory Address Bus
SRAS#	O 2.5V - M	SDRAM Row Address Strobe
SCAS#	O 2.5V - M	SDRAM Column Address Strobe
SWE#	O 2.5V - M	SDRAM Write Enable
CS[5:0]#	O 2.5V - M	SDRAM Chip Select CS[5:0]# multiplexed with DQS[5:0]
DQM#[7:0]	O 2.5V - M	SDRAM Input/Output Data Mask
DQS[7:0]	I/O 2.5V - M	2.5V - M DDR Data Strobe
MD[63:0]	I/O 2.5V - M	System Memory Data Bus
CKE[5:0]	O 2.5V – AUX	SDRAM Clock Enable
S3AUXSW#	O (open-drain) 2.5V - AUX	Aux power switch for ACPI-S3 state, low active.
DDRVREF[A:B]	I M	DDR I/O Reference Voltage
DDRCOMP_P	I M	P-MOS Compensation Input
DDRCOMP_N	I M	N-MOS Compensation Input

5.2 SiS M661FX (IGUI Host Memory Controller) - 3

AGP Interface

Ball Name	Ball Attr	Description
AGPCLK	I 3.3V – M	AGP Clock
AFRAME#	I/O 1.5V - M	AGP Frame#
AIRDY#	I/O 1.5V - M	AGP Initiator Ready
ATRDY#	I/O 1.5V - M	AGP Target Ready
ASTOP#	I/O 1.5V - M	AGP Stop#
ADEVSEL#	I/O 1.5V - M	AGP Device Select
ASERR#	I 1.5V - M	AGP System Error
AREQ#	I 1.5V - M	AGP Bus Request
AGNT#	O 1.5V - M	AGP Bus Grant
ADBI_LO	I/O 1.5V - M	DBI of AAD[15:0]
AAD[31:0]	I/O 1.5V - M	AGP Address/Data Bus
AC/BE[3:0]#	I/O 1.5V - M	AGP Command/Byte Enable
APAR	I/O 1.5V - M	AGP Parity
ST[2:0]	O 1.5V - M	AGP Status Bus
PIPE#	I 1.5V - M	AGP Pipeline Request in v2.0 DBI of AAD[31:16] in v3.0
SBA[7:0]	I/O 1.5V - M	Side Band Address
RBF#	I 1.5V - M	Read Buffer Full
WBF#	I 1.5V - M	Write Buffer Full

AGP Interface (Continued)

Ball Name	Ball Attr	Description
AD_STB[1:0]	I/O 1.5V - M	AD Bus Strobe
AD_STB[1:0]#	I/O 1.5V - M	AD Bus Strobe Compliment
SB_STB	I 1.5V - M	Side Band Strobe
SB_STB#	I 1.5V - M	Side Band Strobe Compliment
GC_DET#	I 1.5V - M	AGP v3.0 strap
AGPCOMP_P	I M	P-MOS Compensation Input
AGPCOMP_N	I M	N-MOS Compensation Input
AGPVREF	I M	AGP Reference Voltage

Stereo Glasses interface

Ball Name	Ball Attr	Description
CSYNC	O 3.3V - M	Reserved
RSYNC	O 3.3V - M	Reserved
LSYNC	O 3.3V - M	Reserved

5.2 SiS M661FX (IGUI Host Memory Controller) - 4

Digital Video Link Interface

Ball Name	Ball Attr	Description
VBCLK	I 1.8V - M	Channel B/A Clock Input VBCLK multiplexed with SBA0
VBHCLK	O 1.8V - M	VB Programming Interface Clock VBHCLK multiplexed with RBF#
VBCAD	I/O 1.8V - M	VB Programming Interface Data VBCAD multiplexed with AREQ#
VBCTL[1:0]	O 1.8V -M	VB Data Control VBCTL[1:0] multiplexed with AAD[29:28]
VGPIO[3:2]	I/O 1.8V - M	VB GPIO pins VGPIO[3:2] multiplexed with IPE#/WBF#
VBHSYNC	I/O 1.8V - M	Channel B H-Sync VBHSYNC multiplexed with AAD30
VBVSYNC	I/O 1.8V - M	Channel B V-Sync VBVSYNC multiplexed with AAD31
VBDE	I/O 1.8V - M	Channel B Data Valid VBDE multiplexed with AAD27
VBGCLK	I/O 1.8V - M	Channel B Clock Output. This clock is used to trigger dual edge data transfer. Perfect duty cycle is required. VBGCLK multiplexed with AD_STB1
VBGCLK#	I/O 1.8V - M	Channel B Differential Clock Output. (To support Chrontel). VBGCLK# multiplexed with AD_STB1#
VBD[11:0]	I/O 1.8V - M	Channel B Data VBD[11:0] multiplexed with AAD
VAHSYNC	I/O 1.8V - M	Channel A H-Sync VAHSYNC multiplexed with AAD18
VAVSYNC	I/O 1.8V - M	Channel A V-Sync VAVSYNC multiplexed with AAD17
VADE	I/O 1.8V - M	Channel A Data Valid VADE multiplexed with AAD16
VAGCLK	I/O 1.8V - M	Channel A Clock Output. This clock is used to trigger dual edge data 1.8V – M transfer. Perfect duty cycle is required. VAGCLK multiplexed with AD_STB0
VAGCLK#	I/O 1.8V - M	Channel A Differential Clock Output. (To support Chrontel). VAGCLK# multiplexed with AD_STB0#
VAD[11:0]	I/O 1.8V - M	Channel A Data VAD[11:0] multiplexed with AAD

Test Mode / Hardware Trap / Power Management

Ball Name	Ball Attr	Description
DLLEN#	I/O 3.3V/5V– M	Hardware Trap pin (refer to section 5)
TRAP2	I 3.3V/5V– AUX	Hardware Trap pin (refer to section 5)
TRAP[1:0]	I 3.3V/5V– M	Hardware Trap pins (refer to section 5)
ENTEST	I 3.3V/5V– M	Test Mode enable pin
TESTMODE[2:0]	I 3.3V/5V– M	Test Mode select pin Nand Tree Test: 100
AUXOK	I 3.3V – AUXI	Auxiliary Power OK : This signal is supplied from the power source of resume well. It is also used to reset the logic in resume power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PCIRST#	I 3.3V – AUXI	PCI Bus Reset : PCIRST# is supplied from SiS963 MuTIOL ? ?G Media IO.
PWROK	I 3.3V – AUXI	Main Power OK : A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, CPURST and PCIRST# will all be asserted until after PWROK goes high for 24 ms.

5.2 SiS M661FX (IGUI Host Memory Controller) - 5

VGA interface

Ball Name	Ball Attr	Description
VOSCI	I 3.3V - M	14.318MHzReference Clock Input
HSYNC	O 3.3V – M	Horizontal Sync
VSYNC	O 3.3V - M	Vertical Sync
INTA#	O 3.3V – M	Internal VGA Interrupt Pin
VGPIO[1:0]	I/O 3.3V/5V- M	Internal VGA GPIO pins
VCOMP	AI Analog - M	Compensation Pin
VRSET	AI Analog - M	Reference Resistor
VVBWN	AI Analog - M	Voltage Reference
ROUT	AO Analog - M	Red Signal Output
GOUT	AO Analog - M	Green Signal Output
BOUT	AO Analog - M	Blue Signal Output

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 1

Host Bus Interface

Name	Pin Attr	Description
FERR#	I 0.8V/2.65V -M	**Floating Point Error:** CPU will assert this signal upon a floating point error occurring.
IGNNE#	OD 0.8V/2.65V -M	**Ignore Numeric Error:** IGNNE# is asserted to inform CPU to ignore a numeric error.
NMI	OD 0.8V/2.65V -M	**Non-Maskable Interrupt:** A rising edge on NMI will trigger a non-maskable interrupt to CPU.
INTR	OD 0.8V/2.65V -M	**Interrupt Request:** High-level voltage of this signal conveys to CPU that there is outstanding interrupt(s) needed to be serviced.
APICD1 / **GPIOFF#** **APICD0 /** **THERM2#**	I/OD I I/OD I 0.8V/2.65V -M	**APIC Data: APICD[1:0]** These two signals are used to send and receive APIC data. **GPIO OFF:** Turn off the system when input a low level signal. **Thermal 2:** Assert a SMI#/SCI# when input a low level signal.
CPUSLP#	OD 0.8V/2.65V -M	**CPU Sleep:** The CPUSLP# can be used to force CPU enter the Sleep state.
STPCLK#	OD 0.8V/2.65V -M	**Stop Clock:** STPCLK# will be asserted to inhibit or throttle CPU activities upon a pre-defined power management event occurs.
SMI#	OD 0.8V/2.65V -M	**System Management Interrupt:** SMI# will be asserted when a pre-defined power management event occurs.
INIT#	OD 0.8V/2.65V -M	**Initialization:** INIT is used to re-start the CPU without flushing its internal caches and registers. In Pentium III platform it is active high. This signal requires an external pull-up resistor tied to VTT.
APICCK/ **LDTREQ# /** **AGPBUSY#**	I 2.5V/3.3V -M	**APIC Clock:** This signal is used to determine when valid data is being sent over the APCI bus. **LDTREQ# / AGPBUSY# (LDTREQ# for K8 use only)** When a low active signal inputs, it will wake up system from C3/S1.
A20M#	OD 0.8V/2.65V- M	**Address 20 Mask:** When A20M# is asserted, the CPU A20 signal will be forced to “0”

MuTIOL 1G Connect Interface

Name	Pin Attr	Description
ZCLK	I 3.3V - M	MuTIOL 1G I/O Connect Clock
ZUREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZDREQ	I/O 1.8V - M	MuTIOL 1G I/O Conect Controll pins
ZSTB[1:0]	I/O 1.8V - M	MuTIOL 1G I/O Connect Strobe
ZSTB[1:0]#	I/O 1.8V - M	MuTIOL 1G Strobe Compliment
ZAD[16:0]	I/O 1.8V - M	MuTIOL 1G Address/Data pins
ZVREF	I -M	MuTIOL 1G I/O reference voltage
ZCMP_N	I -M	MuTIOL 1G N-MOS Compensation Input
ZCMP_P	I -M	MuTIOL 1G P-MOS Compensation input

LPC Interface

Name	Pin Attr	Description
LAD[3:0]	I/O 3.3V/5V-M	**LPC Address/Data Bus:** LPC controller drives these four pins to transmit LPC command, address, and data to LPC device.
LDRQ#	I 3.3V/5V-M	**LPC DMA Request 0:** This pin is used by LPC device to request DMA cycle.
LDRQ1# **(GPIO1)**	I 3.3V/5V-M	**LPC DMA Request 1:** This pin is used by LPC device to request DMA cycle.
LFRAME#	O 3.3V -M	**LPC Frame:** This pin is used to notify LPC device that a start or a abort LPC cycle will occur.
SIRQ	I/O 3.3V/5V -M	**Serial IRQ:** This signal is used as the serial IRQ line signal.

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 2

PCI Interface

Name	Pin Attr	Description
PCICLK	I 3.3V/5V -M	**PCI Clock:** The PCICLK input provides the fundamental timing and the internal operating frequency for the SiS963L. It runs at the same frequency and skew of the PCI local bus.
C/BE[3:0]#	I/O 3.3V/5V -M	**PCI Bus Command and Byte Enables:** PCI Bus Command and Byte Enables define the PCI command during the address phase of a PCI cycle, and the PCI byte enables during the data phases. C/BE[3:0]# are outputs when the SiS963L is a PCI bus master and inputs when it is a PCI slave.
PLOCK#	I/O 3.3V/5V -M	**PCI Lock:** When PLOCK# is sampled asserted at the beginning of a PCI cycle, SiS963L considers itself being locked and remains in the locked state until PLOCK# is sampled and negated at the following PCI cycle.
AD[31:0]	I/O 3.3V/5V -M	**PCI Address /Data Bus:** In address phase: 1.When the SiS963L is a PCI bus master, AD[31:0] are output signals. 2.When the SiS963L is a PCI target, AD[31:0] are input signals. In data phase: 1.When the SiS963L is a target of a memory read/write cycle, AD[31:0] are floating. 2.When the SiS963L is a target of a configuration or an I/O cycle, AD[31:0] are output signals in a read cycle, and input signals in a write cycle.
PAR	I/O 3.3V/5V -M	**Parity:** SiS963L drives out Even Parity covering AD[31:0] and C/BE[3:0]#. It does not check the input parity signal.
IRDY#	I/O 3.3V/5V -M	**Initiator Ready:** IRDY# is an output when the SiS963L is a PCI bus master. The assertion of IRDY# indicates the current PCI bus master's ability to complete the current data phase of the transaction. For a read cycle, IRDY# indicates that the PCI bus master is prepared to accept the read data on the following rising edge of the PCI clock. For a write cycle, IRDY# indicates that the bus master has driven valid data on the PCI bus. When the SiS963L is a PCI slave, IRDY# is an input pin.

PCI Interface (Continued)

Name	Pin Attr	Description
FRAME#	I/O 3.3V/5V -M	**Frame#:**FRAME# is an output when the SiS963L is a PCI bus master. The SiS963L drives FRAME# to indicate the beginning and duration of an access. When the SiS963L is a PCI slave device, FRAME# is an input signal.
TRDY#	I/O 3.3V/5V -M	**Target Ready:** TRDY# is an output when the SiS963L is a PCI slave. The assertion of TRDY# indicates the target agent's ability to complete the current data phase of the transaction. For a read cycle, TRDY# indicates that the target has driven valid data onto the PCI bus. For a write cycle, TRDY# indicates that the target is prepared to accept data from the PCI bus. When the SiS963L is a PCI master, it is an input pin.
STOP#	I/O 3.3V/5V -M	**Stop#:**STOP# indicates that the bus master must start terminating its current PCI bus cycle at the next clock edge and release control of the PCI bus. STOP# is used for disconnection, retry, and target-abortion sequences on the PCI bus.
DEVSEL#	I/O 3.3V/5V -M	**Device Select:** As a PCI target, SiS963L asserts DEVSEL# by doing positive or subtractive decoding. SiS963L positively asserts DEVSEL# when the DRAM address is being accessed by a PCI master, PCI configuration registers or embedded controllers' registers are being addressed, or the BIOS memory space is being accessed. The low 16K I/O space and low 16M memory space are responded subtractively. The DEVESEL# is an input pin when SiS963L is acting as a PCI master. It is asserted by the addressed agent to claim the current transaction.
PREQ[4:0]#	I 3.3V/5V -M	**PCI Bus Request:** PCI Bus Master Request Signals
PGNT[4:0]#	O 3.3V –M	**PCI Bus Grant:** PCI Bus Master Grant Signals
PREQ5# / GPIO5	I I/O 3.3V/5V- M	**PCI Bus Request:** PCI Bus Master Request Signal

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 3

PCI Interface (Continued)

Name	Pin Attr	Description
PGNT5# / GPIO6	O I/O 3.3V- M	**PCI Bus Grant:** PCI Bus Master Grant Signal
INT[A:D]#	I 3.3V/5V –M	**PCI interrupt A,B,C,D:** The PCI interrupts will be connected to the inputs of the internal Interrupt controller through the rerouting logic associated with each PCI interrupt.
PCIRST#	O 3.3V –M	**PCI Bus Reset:** PCIRST# will be asserted during the period when PWROK is low, and will be kept on asserting until about 24ms after PWROK goes high.
SERR#	I 3.3V/5V –M	**System Error:** When sampled active low, a non-maskable interrupt (NMI) can be generated to CPU if enabled.

Keyboard Controller Interface

Name	Pin Attr	Description
KBDAT (GPIO15)	I/OD 3.3V/5V -AUX	**Keyboard Dada:** When the internal keyboard controller is enabled, this pin is used as the keyboard data signal.
KBCLK (GPIO16)	I/OD 3.3V/5V -AUX	**Keyboard Clock:** When the internal keyboard controller is enabled, this pin is used as the keyboard clock signal.
PMDAT (GPIO17)	I/OD 3.3V/5V -AUX	**PS2 Mouse Data:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as PS2 mouse data signal.
PMCLK (GPIO18)	I/OD 3.3V/5V -AUX	**PS2 Mouse Clock:** When the internal keyboard and PS2 mouse controllers are enabled, this pin is used as the PS2 mouse clock signal.

IDE Interface

Name	Pin Attr	Description
IDA[15:0]	I/O 3.3V/5V -M	Primary Channel Data Bus
IDB[15:0]	I/O 3.3V/5V -M	Secondary Channel Data Bus
IDECSA[1:0]#	O 3.3V -M	Primary Channel CS[1:0]
IDECSB[1:0]#	O 3.3V -M	Secondary Channel CS[1:0]
IIOR[A:B]#	O 3.3V -M	Primary/Secondary Channel IOR# Signals
IIOW[A:B]#	O 3.3V -M	Primary/Secondary Channel IOW# Signals
ICHRDY[A:B]	I 3.3V/5V -M	Primary/Secondary Channel ICHRDY# Signals
IDREQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel DMA Request Signals
IDACK[A:B]#	O 3.3V -M	Primary/Secondary Channel DMACK# Signals
IIRQ[A:B]	I 3.3V/5V -M	Primary/Secondary Channel Interrupt Signals
IDSAA[2:0]	O 3.3V -M	Primary Channel Address [2:0]
IDSAB[2:0]	O 3.3V -M	Secondary Channel Address [2:0]
CBLID[A:B]	I 3.3V/5V -M	Primary/Secondary Ultra-66 Cable ID

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 4

Power Management Interface

Name	Pin Attr	Description
ACPILED	OD <=5V -AUX	**ACPILED :** ACPILED can be used to control the blinking of an LED at the frequency of 1 Hz to indicate the system is at power saving mode.
EXTSMI# (GPIO3)	I I/O 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
PME#	I 3.3V/5V -AUX	**PME# :** When the system is in power-down mode, an active low event on PME# will cause the PSON# to go low and hence turn on the power supply. When the system is in suspend mode, an active PME# event will cause the system wakeup and generate an SCI/SMI#.
PSON#	OD <=5V -AUX	**ATX Power ON/OFF control:** PSON# is used to control the on/off state of the ATX power supply. When the ATX power supply is in the OFF state, an activated power-on event will force the power supply to ON state.
AUXOK	I 3.3V -AUX	**Auxiliary Power OK:** This signal is supplied from the AUX power source. It is also used to reset the logic in AUX power well. If there is no auxiliary power source on the system, this pin should be tied together with PWROK.
PWRBTN#	I 3.3V/5V -AUX	**Power Button:** This signal is from the power button switch and will be monitored by the ACPI-compatible power management unit to switch the system between working and sleeping states.
THERM# (GPIO2)	I 3.3V/5V -M	**Thermal Alarm:** When a low active signal inputs, it will assert a SMI#/SCI# event and assert CPU throttling.
EXTSMI# (GPIO3)	I 3.3V/5V -M	**External SMI#:** EXTSMI# can be used to generate wakeup event, sleep event, or SCI/SMI# event to the ACPI compatible power management unit.
CLKRUN# (GPIO4)	I/O 3.3V/5V –M	**Clock Run: (for Mobile only)** Used by PCI and LPC peripherals to request the system PCI clock to re-start, or prevent PCI clock stopping. An external pull-up to the MAIN power is required.

Power Management Interface (Continued)

Name	Pin Attr	Description
GPWAK# (GPIO7)	I 3.3V/5V -AUX	**General Purpose Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
RING (GPIO8)	I 3.3V/5V -AUX	**Ring Indication:** An active RING pulse and lasting for more than 4ms will cause a wakeup event for system to wake from S1~S5.
AC_SDIN2, 3 (GPIO9, 10)	I 3.3V/5V -AUX	**AUDIO Wake-Up Signal:** Used to wake up the system from S1/S3/S4/S5.
STP_PCI# / AGPSTOP# (GPIO11)	O OD 3.3V/5V –AUX	**Stop PCI Clock: (for Mobile only)** Used to stop the system PCI clock. Used to support PCI CLKRUN# protocol. **AGP Clock Stop: (for Mobile only, if GPIO14 is used to be S3AUXSW#)** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state.
CPUSTP# (GPIO12)	OD 1.5V/5V -AUX	**CPU Clock Stop (for Mobile only):** For Intel Mobile processor, this signal can be used to stop the clock to the processor. This signal connected to the DPSLP# signal of Pentium 4 processor that can let the processor enter the Deep Sleep state as well (recommended). For AMD processor, this signal can be to reduce processor voltage during C3/S1 state.
DPRSLPVR (GPIO13)	O 3.3V/5V -AUX	**Deeper Sleep (for Mobile only):** Used to lower the voltage of VRM during CPU entered the deeper power saving mode. Because this signal will be at input mode after the Clear RTC operation, an external pulled down resistor is required for this signal. When this signal is high, the voltage regulator outputs the Deeper Sleep voltage. When this signal is low (default), the voltage regulator output the Normal voltage. DPRSLP# can be used to lower the Intel processor voltage during C3/S1 state.
AGPSTOP# / S3AUXSW# (GPIO14)	OD 3.3V/5V -AUX	**AGP Clock Stop (for Mobile only):** AGPSTOP# is used to stop the AGP_CLOCK output from clock generator during C3/S1 state. **S3AUXSW#:(for SiS755 and SiSR658 use only)** The signal will keep low in S3 state.

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 5

Power Management Interface (Continued)

Name	Pin Attr	Description
VR_HILO# (GPIO15)	O 3.3V/5V -AUX	**Voltage Regulator HI / LO (for Mobile only):** This ping is used to select an appropriate VID for voltage regulator. A low level indicates the Battery Optimal mode. A high level indicates the Maximum Performance mode.
LO_HI# (GPIO16)	OD 1.5V/5V -AUX	**LO_HI# (for Mobile only):** This pin is connected to the processor. A high level indicates the Battery Optimal mode. A low level indicates the Maximum Performance mode.
VGATEM# (GPIO17)	OD 1.5V/5V -AUX	**VGATEM# (for Mobile only):** Output pin, it is used to mask the PWRGOOD of processor core voltage regulator.
RTC32KHZ (GPIO18)	O 3.3V/5V -AUX	**RTC32KHz output: (Mobile only)** Support RTC32KHz clock output in S0~S5.
THERM2# (APICD0)	I 0.8V/2.65V -M	**Thermal Alarm2: (GTL level)** When a low active signal inputs, it will assert a SMI#/SCI# event.
GPIOFF# (APICD1)	I 0.8V/2.65V -M	**GPIO OFF: (GTL level)** When a low level signal inputs, it will turn off the system. Then, the system can only be woken up again by PWRBTN#.

RTC Interface

Name	Pin Attr	Description
BATOK	I 3.3V -RTC	**Battery Power OK:** When the internal RTC is enabled, this signal is used to indicate that the power of RTC well is stable. It is also used to reset the logic in RTC well. If the internal RTC is disabled, this pin should be tied low.
OSC32KHI	I 3.3V-RTC	**RTC 32.768 KHz Input:** When internal RTC is enabled, this pin provides the 32.768 KHz clock signal from external crystal or oscillator.
OSC32KHO	O 3.3V -RTC	**RTC 32.768 KHz Output:** When internal RTC is enabled, this pin should be connected with the other end of the 32.768 KHz crystal or left unconnected if an external oscillator is used.
PWROK	I 3.3V-RTC	**Main Power** OK: A high-level input to this signal indicates the power being supplied to the system is in stable operating state. During the period of PWROK being low, PCIRST# will all be asserted until after PWROK goes high for 12 ms.

General Purpose I/O

Name	Pin Attr	Description
GPIO[6:0]	I/O 3.3V/5V -M	**GPIO:** Can be a General Purpose Input or Output.
GPIO[15:7]	I/O 3.3V/5V - AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[18:16]	O 3.3V/5V – AUX	**GPO:** Can be a General Purpose Output.
GPIO[20:19]	OD 3.3V/5V – AUX	**GPIO:** Can be a General Purpose Input or Output.
GPIO[24:21]	I 3.3V/5V - AUX	**GPI:** Can be a General Purpose Input.

Hardware Trap Signals

Name	Pin Attr	Description
IPB_OUT0	O 3.3V -AUX	**IPB_OUTO:** Hardware Trap to select MuTIOL 1G clock PLL enable/disable
IPB_OUT1	O 3.3V – AUX	**IPB_OUT1:** Hardware Trap to select MuTIOL 1G operation mode

5.3 SiS963L(MuTIOL®Media I/O South Bridge) - 6

AC’97 Interface

Name	Pin Attr	Description
AC_BIT_CLK	I 3.3V/5V -M	**AC’97 Bit Clock:** This signal is a 12.288MHz serial data clock, which is generated by primary Codec.
AC_RESET#	O 3.3V -AUX	**AC’97 Reset:** Hardware reset signal for external Codecs.
AC_SDIN0	I 3.3V/5V -AUX	**AC’97 Serial Data Input :** Serial data input from primary Codec.
AC_SDIN1	I 3.3V/5V -AUX	**AC’97 Serial Data Input:** Serial data input from secondary Codec. When Modem Codec is used, this pin dedicate to Modem Serial data input.
AC_SDIN[3:2] **(GPIO[10:9])**	I 3.3V/5V -AUX	**AC’97 Serial Data Input:** Serial data input from third and forth Audio Codec.
AC_SDOUT	O 3.3V -M	**AC’97 Serial Data Output:** Serial data output to Codecs.
AC_SYNC	O 3.3V -M	**AC’97 Synchronization:** This is a 48KHz signal, which is used to synchronize the Codecs.

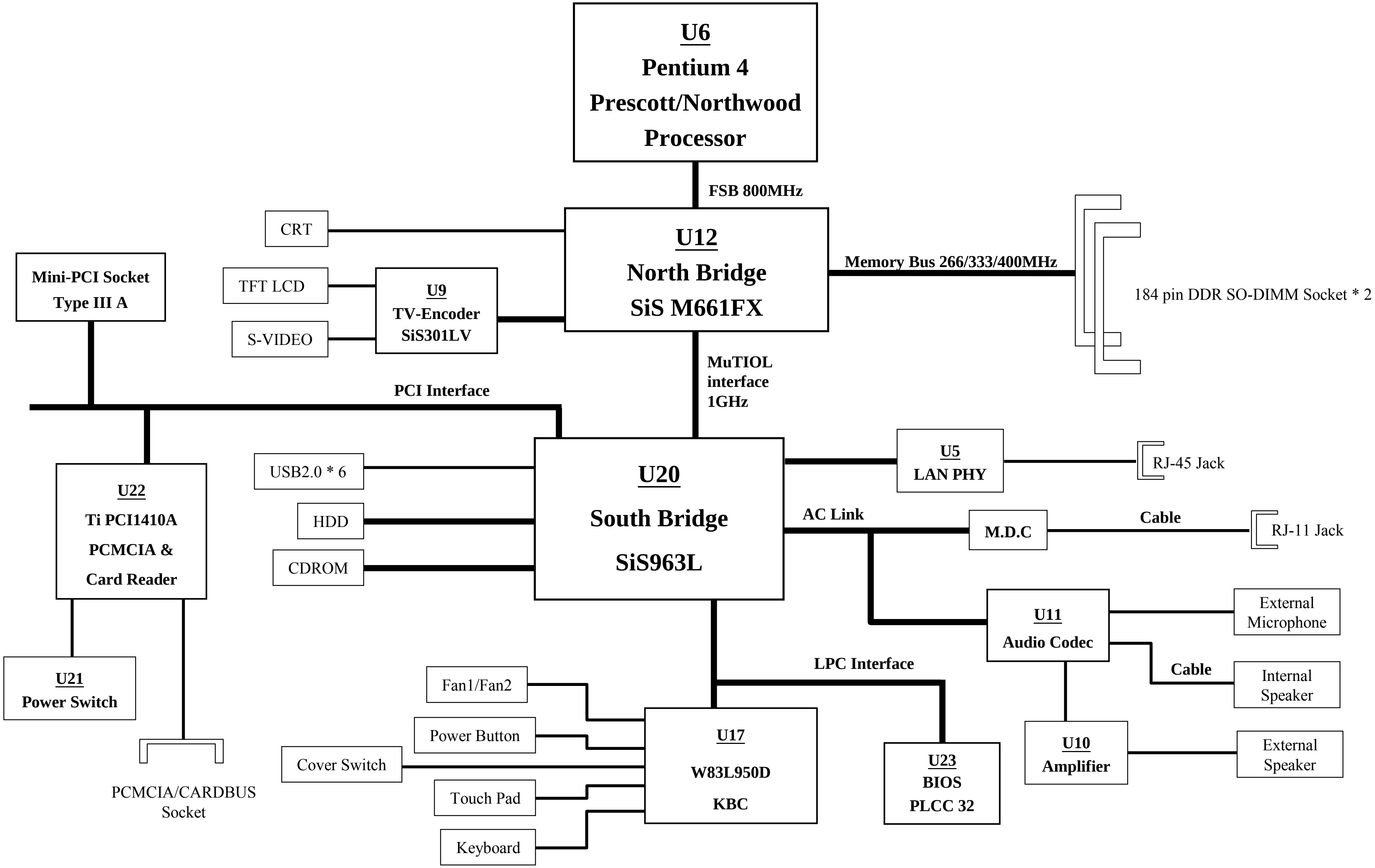
Legacy I/O and Miscellaneous Signals

Name	Pin Attr	Description
SPK	O 3.3V -M	**Speaker output:** The SPK is connected to the system speaker.
ENTEST	I 3.3V/5V -M	SiS963L Test Mode Enable Pin
OSCI	I 3.3V -M	14.318 MHz. Clock In

USB Interface

Name	Pin Attr	Description
OSC12MHI	I 3.3V/5V -AUX	**UTMI 12MHz Clock Input:** This pin provides the 12MHz clock signal input form external crystal or oscillator.
OSC12MHO	O 3.3V/5V -AUX	**UTMI 12Mhz Clock Output:** **This pin should be connected with the other end of the 12Mhz crystal or left unconnected if an external oscillator is used**
USBCLK48M	I 3.3V/5V -M	**USB 48 MHz clock input:** This signal provides the fundamental clock for the USB Controller.
OC[0:5]#	I/O 3.3V/5V - AUX	**USB Port 0-5 Overcurrent Detection:** OC[0:5]# are used to detect the overcurrent condition of USB Ports 0-5.
UV[3,0]+, **UV[3,0]-**	I/O 3.3V - AUX	**USB Port [3:**0] **Differentia**l: These differential pairs are used to transmit Data/Address /Command signals for ports 3 and 0. (USB controller 0)
UV[4,1]+, **UV[4,1]-**	I/O 3.3V - AUX	**USB Port [4:1] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 4 and 1. (USB controller 1)
UV[5,2]+, **UV[5,2]-**	I/O 3.3V - AUX	**USB Port [5,2] Differentia**l: These differential pairs are used to transmit Data/Address/Command signals for ports 5 and 2. (USB controller 2)
USBREF	I 3.3V – AUX	**USB reference resistor inpu**t: A resistor should be connected to USBVSS from this pin for IO impedance calibration.

6. System Block Diagram


U6
Pentium 4
Prescott/Northwood
Processor
FSB 800MHz
CRT
U12
North Bridge
SiS M661FX
Memory Bus 266/333/400MHz
184 pin DDR SO-DIMM Socket * 2
Mini-PCI Socket
Type III A
TFT LCD
S-VIDEO
U9
TV-Encoder
SiS301LV
MuTIOL
interface
1GHz
PCI Interface
U20
South Bridge
SiS963L
U5
LAN PHY
RJ-45 Jack
USB2.0 * 6
HDD
CDROM
U22
Ti PCI1410A
PCMCIA &
Card Reader
AC Link
M.D.C
Cable
RJ-11 Jack
U11
Audio Codec
External
Microphone
Cable
Internal
Speaker
LPC Interface
U21
Power Switch
Fan1/Fan2
Power Button
Cover Switch
Touch Pad
Keyboard
U17
W83L950D
KBC
U23
BIOS
PLCC 32
U10
Amplifier
External
Speaker
PCMCIA/CARDBUS
Socket

7. Maintenance Diagnostics

7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot.

7.2 Error Codes (1)

Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
10h	Some type of lone reset
11h	Turn off FAST A20 for POST
12h	Signal power on reset
13h	Initialize the chipset
14h	Search for ISA Bus VGA adapter
15h	Reset counter / Timer 1
16h	User register config through CMOS
17h	Size memory
18h	Dispatch to RAM test
19h	Check sum the ROM
1Ah	Reset PIC’s
1Bh	Initialize video adapter(s)
1Ch	Initialize video (6845Regs)
1Dh	Initialize color adapter
1Eh	Initialize monochrome adapter
1Fh	Test 8237A page registers

Code	POST Routine Description
20h	Test keyboard
21h	Test keyboard controller
22h	Check if CMOS RAM valid
23h	Test battery fail & CMOS X-SUM
24h	Test the DMA controller
25h	Initialize 8237A controller
26h	Initialize int vectors
27h	RAM quick sizing
28h	Protected mode entered safely
29h	RAM test completed
2Ah	Protected mode exit successful
2Bh	Setup shadow
2Ch	Going to initialize video
2Dh	Search for monochrome adapter
2Eh	Search for color adapter
2Fh	Sign on messages displayed

7.2 Error Codes (2)

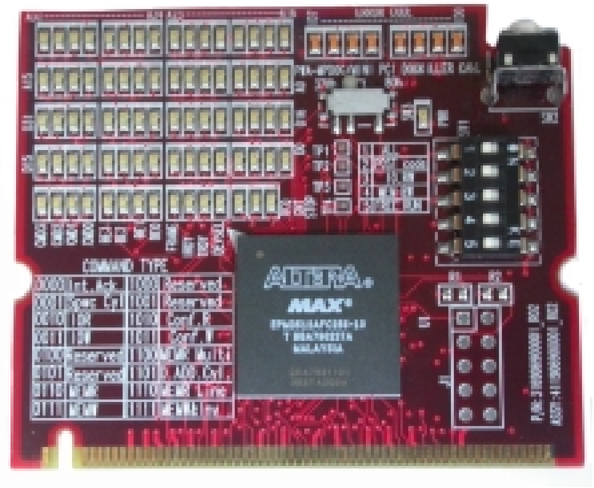
Following is a list of error codes in sequent display on the PIO debug board.

Code	POST Routine Description
30h	Special init of keyboard ctlr
31h	Test if keyboard Present
32h	Test keyboard Interrupt
33h	Test keyboard command byte
34h	Test, blank and count all RAM
35h	Protected mode entered safely(2)
36h	RAM test complete
37h	Protected mode exit successful
38h	Update output port
39h	Setup cache controller
3Ah	Test if 18.2Hz periodic working
3Bh	Test for RTC ticking
3Ch	Initialize the hardware vectors
3Dh	Search and init the mouse
3Eh	Update NUMLOCK status
3Fh	Special init of COMM and LPT ports

Code	POST Routine Description
40h	Configure the COMM and LPT ports
41h	Initialize the floppies
42h	Initialize the hard disk
43h	Initialize option ROMs
44h	OEM's init of power management
45h	Update NUMLOCK status
46h	Test for coprocessor installed
47h	OEM functions before boot
48h	Dispatch to operate system boot
49h	Jump into bootstrap code
50h	ACPI init
51h	PM init & Geyserville CPU init
52h	USB HC init

7.3 Debug Tool

7.3.1 Diagnostic Tool for Mini PCI Slot :



P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 Battery Can not Be Charged
- 8.3 No Display (*2)
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 TV Test Error
- 8.7 Memory Test Error
- 8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.9 Hard Drive Test Error
- 8.10 CD-ROM Driver Test Error
- 8.11 USB Port Test Error
- 8.12 PC Card Socket Test Error
- 8.13 Mini-PCI Socket Test Error
- 8.14 Audio Failure
- 8.15 LAN Test Error

*1: No power definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can’t leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can’t leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

*2: No display definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can’t get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

Keyword:

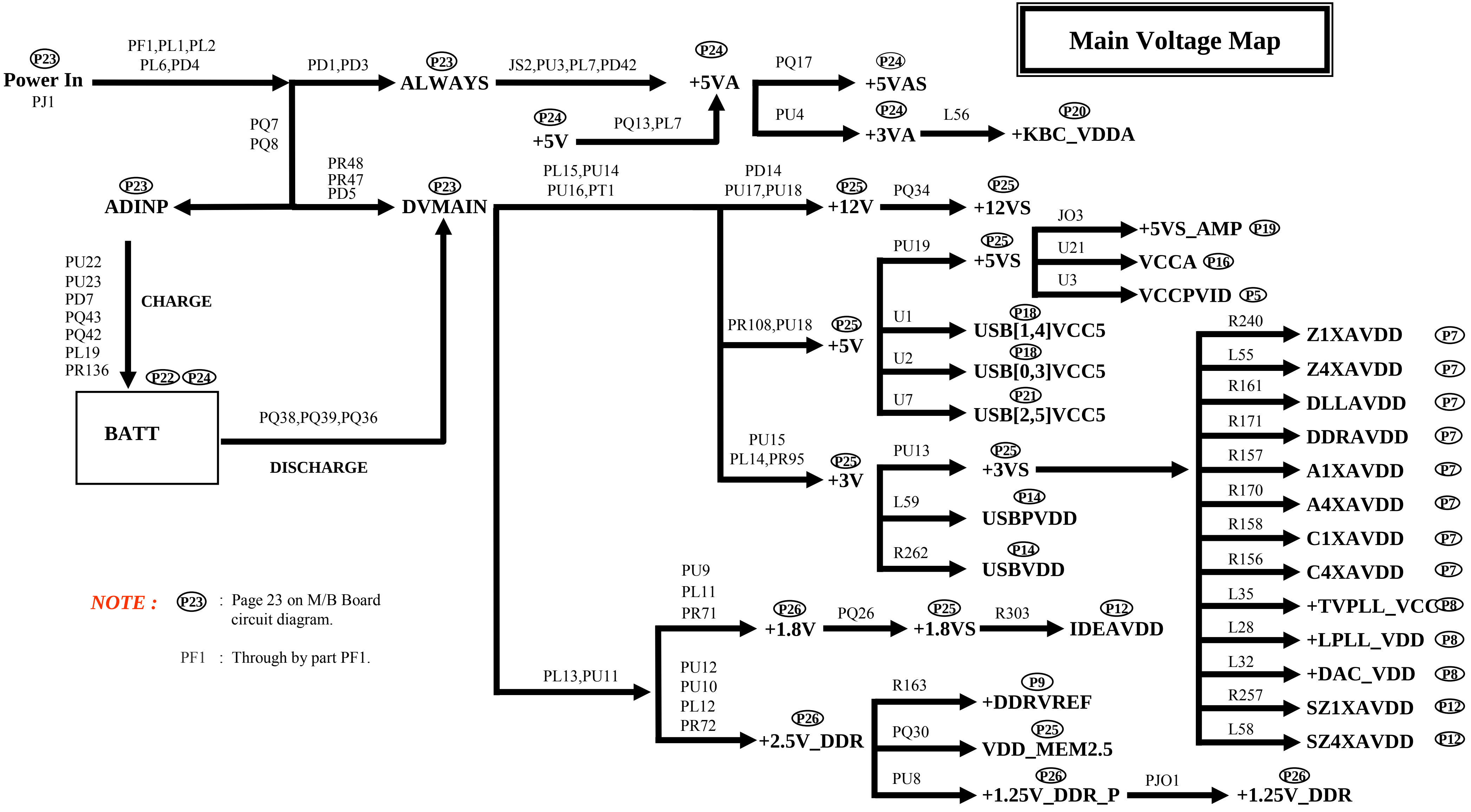
- S5: *Soft Off*
- S0: *Working*

For detail please refer the ACPI specification

8599 N/B Maintenance

8.1 No Power (1)

When power button is pressed ,nothing happens ,power indicator does not light up.

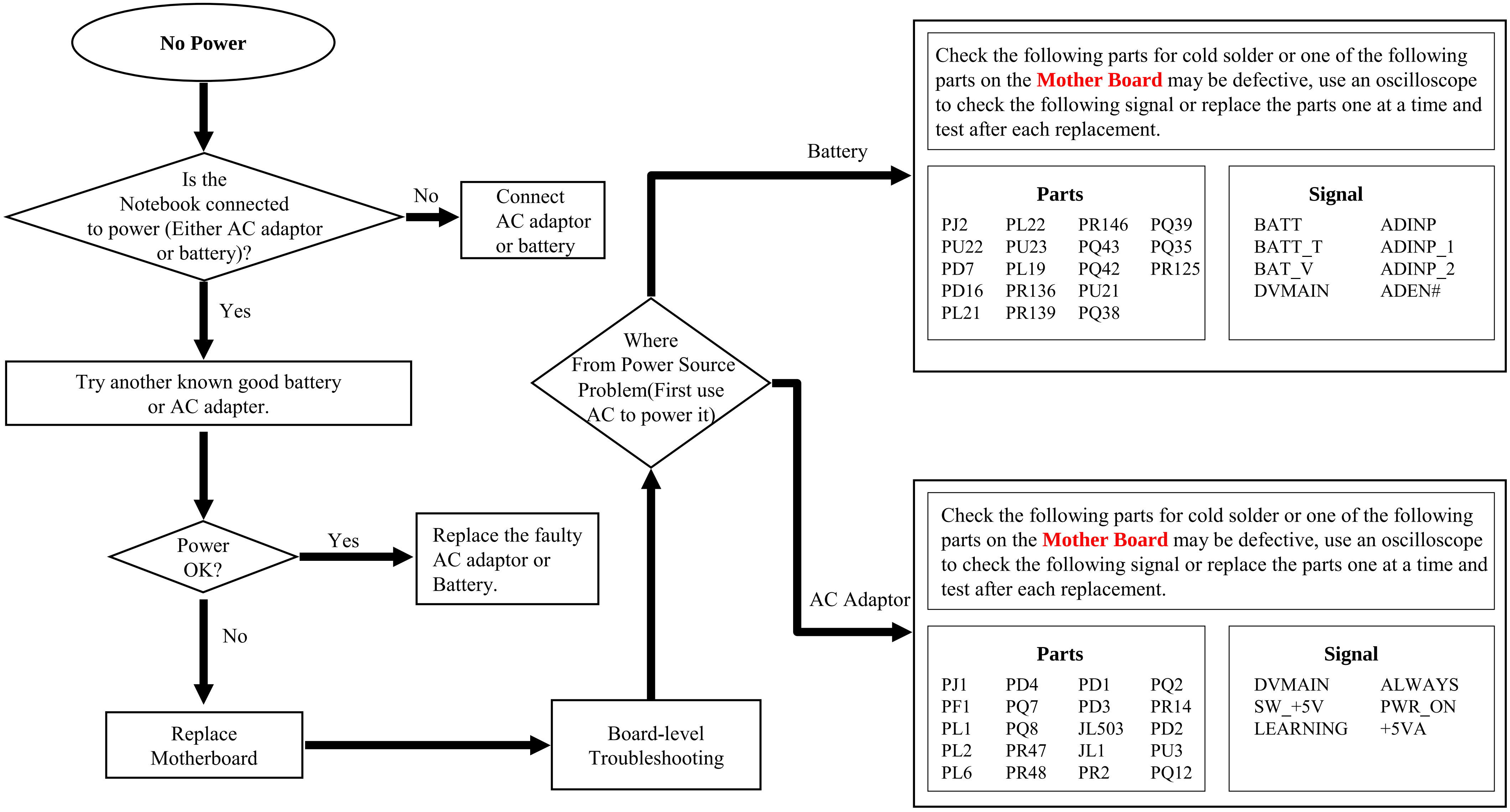

Main Voltage Map
P23
Power In
PJ1
PF1,PL1,PL2
PL6,PD4
PD1,PD3
P23
ALWAYS
JS2,PU3,PL7,PD42
P24
+5VA
PQ17
P24
+5VAS
PU4
P24
+3VA
L56
P20
+KBC_VDDA
P24
+5V
PQ13,PL7
PQ7
PQ8
PR48
PR47
PD5
P23
ADINP
P23
DVMAIN
PL15,PU14
PU16,PT1
PD14
PU17,PU18
P25
+12V
PQ34
P25
+12VS
JO3
+5VS_AMP
P19
U21
VCCA
P16
U3
VCCPVID
P5
PU19
P25
+5VS
PU22
PU23
PD7
PQ43
PQ42
PL19
PR136
CHARGE
P22
P24
BATT
PQ38,PQ39,PQ36
DISCHARGE
PR108,PU18
P25
+5V
U1
P18
USB[1,4]VCC5
U2
P18
USB[0,3]VCC5
U7
P21
USB[2,5]VCC5
PU15
PL14,PR95
P25
+3V
PU13
P25
+3VS
L59
P14
USBPVDD
R262
P14
USBVDD
R240
Z1XAVDD
P7
Z4XAVDD
P7
R161
DLLAVDD
P7
R171
DDRAVDD
P7
R157
A1XAVDD
P7
R170
A4XAVDD
P7
R158
C1XAVDD
P7
R156
C4XAVDD
P7
L35
+TVPLL_VCC
P8
L28
+LPLL_VDD
P8
L32
+DAC_VDD
P8
R257
SZ1XAVDD
P12
L58
SZ4XAVDD
P12
PU9
PL11
PR71
P26
+1.8V
PQ26
P25
+1.8VS
R303
P12
IDEAVDD
PL13,PU11
PU12
PU10
PL12
PR72
P26
+2.5V_DDR
R163
P9
+DDRVREF
PQ30
P25
VDD_MEM2.5
PU8
P26
+1.25V_DDR_P
PJO1
P26
+1.25V_DDR

NOTE : P23 : Page 23 on M/B Board circuit diagram.

PF1 : Through by part PF1.

8.1 No Power (2)

When power button is pressed ,nothing happens ,power indicator does not light up.



No Power

Is the Notebook connected to power (Either AC adaptor or battery)?

No

Connect AC adaptor or battery

Yes

Try another known good battery or AC adapter.

Power OK?

Yes

Replace the faulty AC adaptor or Battery.

No

Replace Motherboard

Board-level Troubleshooting

Where From Power Source Problem(First use AC to power it)

Battery

Check the following parts for cold solder or one of the following parts on the **Mother Board** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts

PJ2
PU22
PD7
PD16
PL21
PL22
PU23
PL19
PR136
PR139
PR146
PQ43
PQ42
PU21
PQ38
PQ39
PQ35
PR125

Signal

BATT
BATT_T
BAT_V
DVMAIN
ADINP
ADINP_1
ADINP_2
ADEN#

AC Adaptor

Check the following parts for cold solder or one of the following parts on the **Mother Board** may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts

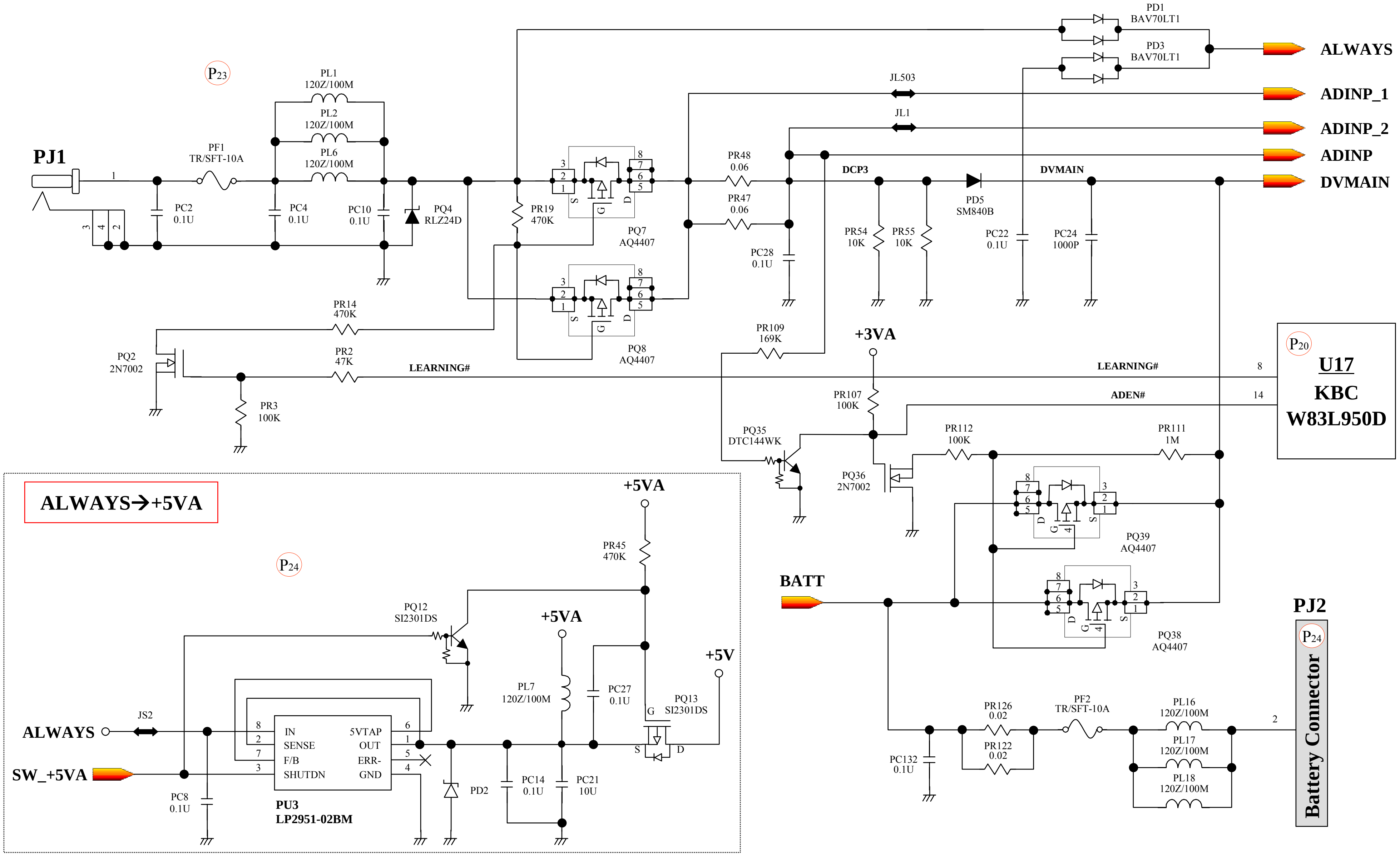
PJ1
PF1
PL1
PL2
PL6
PD4
PQ7
PQ8
PR47
PR48
PD1
PD3
JL503
JL1
PR2
PQ2
PR14
PD2
PU3
PQ12

Signal

DVMAIN
SW_+5V
LEARNING
ALWAYS
PWR_ON
+5VA

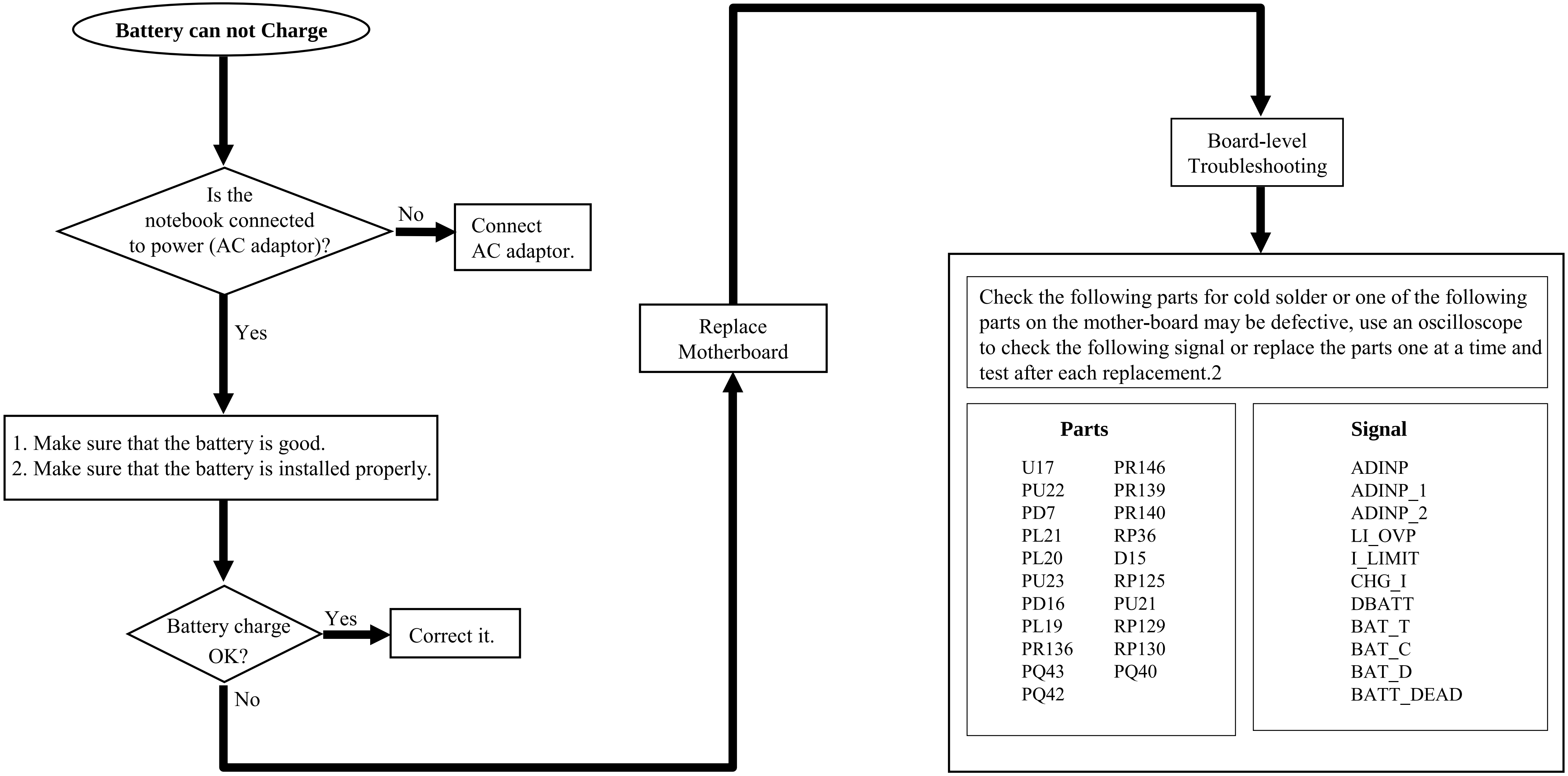
8.1 No Power (3)

When power button is pressed ,nothing happens ,power indicator does not light up.


PD1
BAV70LT1
PD3
BAV70LT1
ALWAYS
JL503
ADINP_1
JL1
ADINP_2
ADINP
DVMAIN
P23
PL1
120Z/100M
PL2
120Z/100M
PL6
120Z/100M
PJ1
PF1
TR/SFT-10A
PC2
0.1U
PC4
0.1U
PC10
0.1U
PQ4
RLZ24D
PR19
470K
PQ7
AQ4407
PQ8
AQ4407
PR48
0.06
PR47
0.06
DCP3
PD5
SM840B
PR54
10K
PR55
10K
PC22
0.1U
PC24
1000P
PC28
0.1U
PR14
470K
PQ2
2N7002
PR2
47K
LEARNING#
PR3
100K
PR109
169K
+3VA
PR107
100K
ADEN#
PQ35
DTC144WK
PR112
100K
PR111
1M
PQ36
2N7002
PQ39
AQ4407
P20
U17
KBC
W83L950D
8
14
BATT
PQ38
AQ4407
PJ2
P24
Battery Connector
PR126
0.02
PR122
0.02
PF2
TR/SFT-10A
PL16
120Z/100M
PL17
120Z/100M
PL18
120Z/100M
PC132
0.1U
2
ALWAYS→+5VA
+5VA
PR45
470K
P24
PQ12
SI2301DS
+5VA
+5V
PL7
120Z/100M
PC27
0.1U
PQ13
SI2301DS
JS2
ALWAYS
SW_+5VA
IN
SENSE
F/B
SHUTDN
5VTAP
OUT
ERR-
GND
PU3
LP2951-02BM
PC8
0.1U
PD2
PC14
0.1U
PC21
10U

8.2 Battery Can not Be Charged (1)

When the battery is installed but the battery status indicate LED display abnormal.


Battery can not Charge
Is the notebook connected to power (AC adaptor)?
No
Connect AC adaptor.
Yes
1. Make sure that the battery is good.
2. Make sure that the battery is installed properly.
Battery charge OK?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.2

Parts

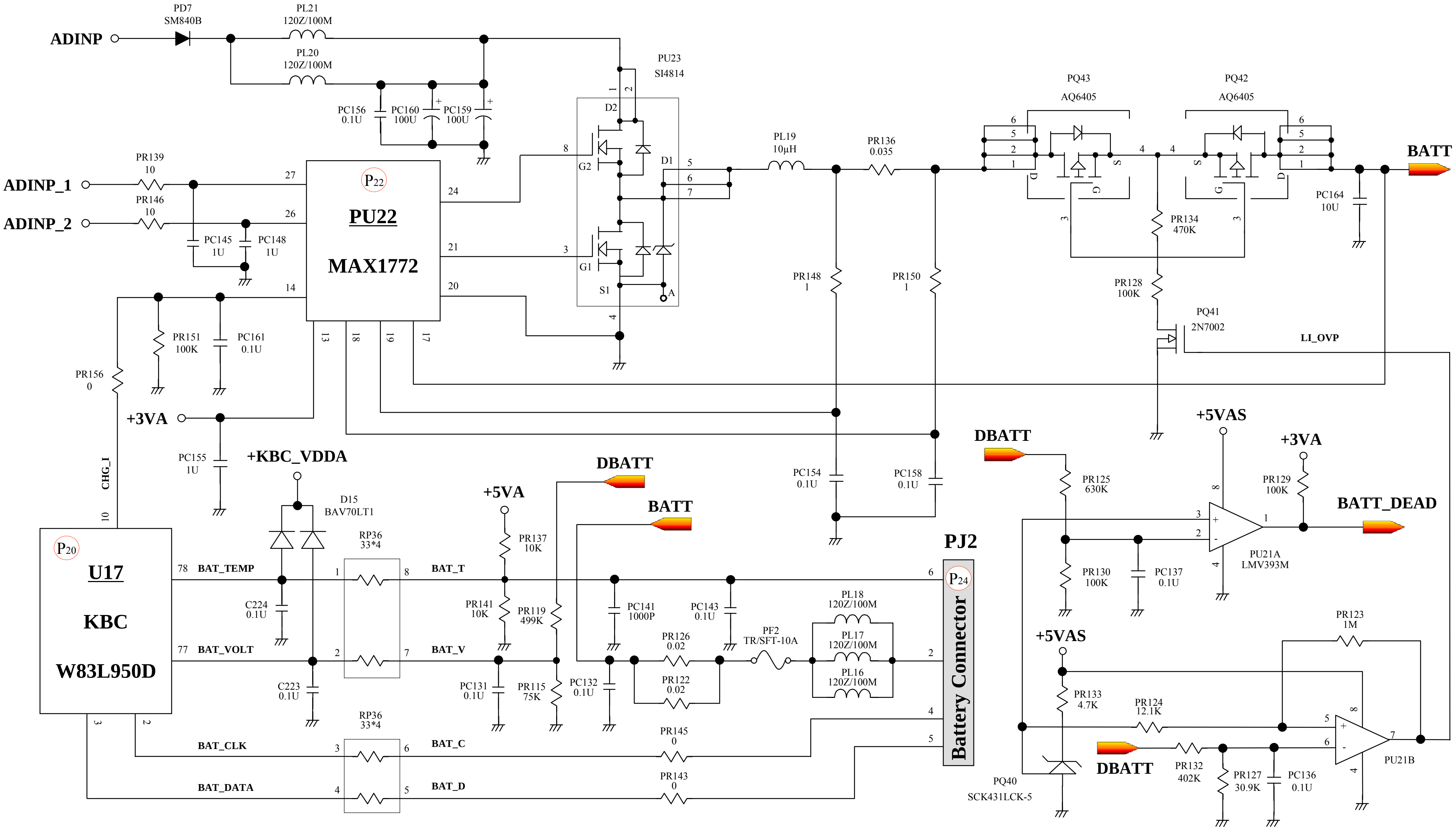
U17
PU22
PD7
PL21
PL20
PU23
PD16
PL19
PR136
PQ43
PQ42
PR146
PR139
PR140
RP36
D15
RP125
PU21
RP129
RP130
PQ40

Signal

ADINP
ADINP_1
ADINP_2
LI_OVP
I_LIMIT
CHG_I
DBATT
BAT_T
BAT_C
BAT_D
BATT_DEAD

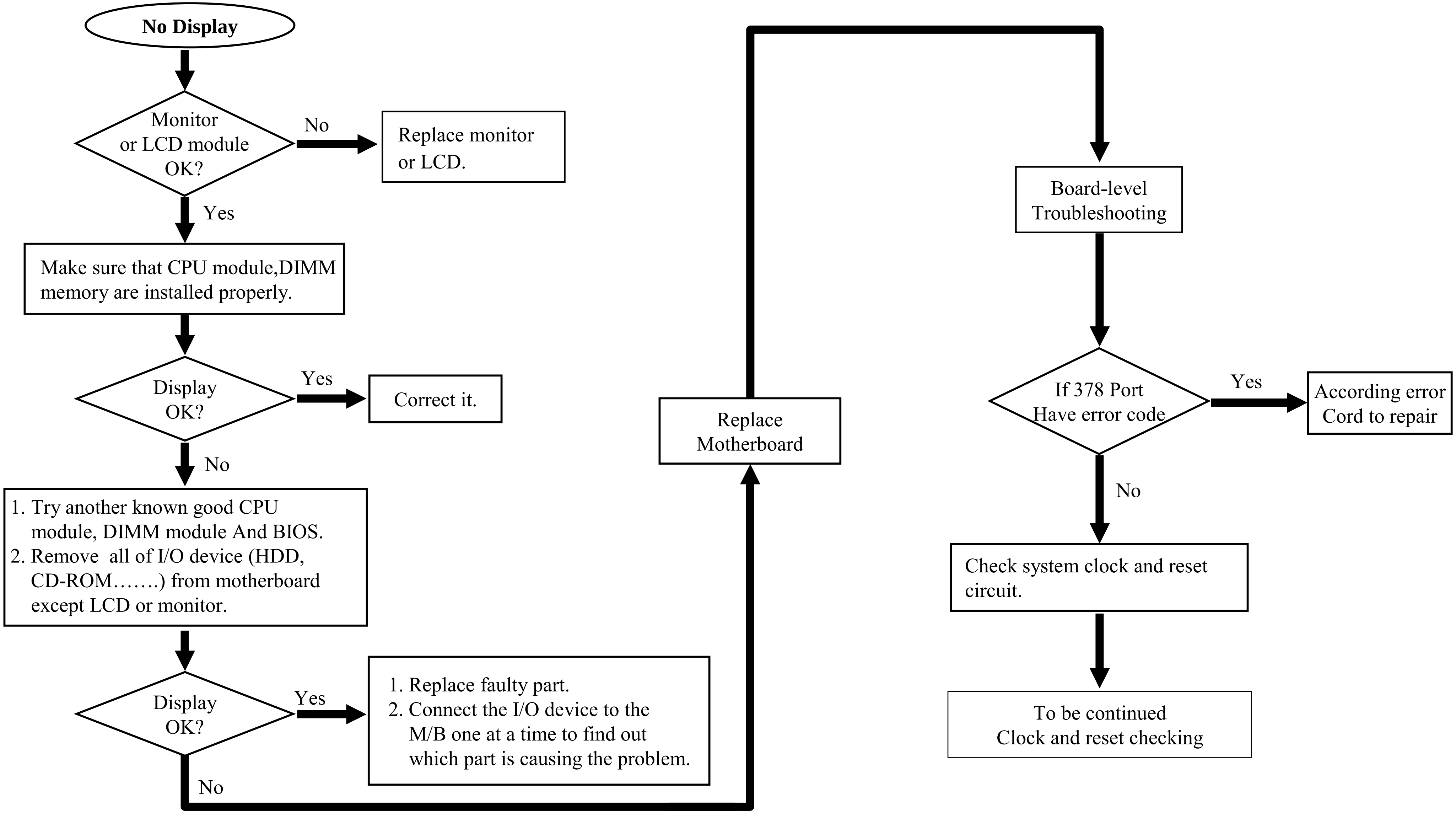
8.2 Battery Can not Be Charged (2)

When the battery is installed but the battery status indicate LED display abnormal.


ADINP
PD7
SM840B
PL21
120Z/100M
PL20
120Z/100M
PC156
0.1U
PC160
100U
PC159
100U
PU23
SI4814
D2
G2
D1
G1
S1
A
PL19
10µH
PR136
0.035
PQ43
AQ6405
PQ42
AQ6405
BATT
PC164
10U
PR134
470K
PR128
100K
PQ41
2N7002
LI_OVP
ADINP_1
PR139
10
ADINP_2
PR146
10
PC145
1U
PC148
1U
P22
PU22
MAX1772
PR151
100K
PC161
0.1U
PR148
1
PR150
1
PR156
0
+3VA
PC155
1U
CHG_I
+KBC_VDDA
D15
BAV70LT1
RP36
33*4
+5VA
PR137
10K
DBATT
BATT
PC154
0.1U
PC158
0.1U
DBATT
PR125
630K
+5VAS
+3VA
PR129
100K
BATT_DEAD
PU21A
LMV393M
PR130
100K
PC137
0.1U
P20
U17
KBC
W83L950D
BAT_TEMP
BAT_VOLT
BAT_CLK
BAT_DATA
C224
0.1U
C223
0.1U
BAT_T
BAT_V
BAT_C
BAT_D
PR141
10K
PR119
499K
PC131
0.1U
PR115
75K
PC132
0.1U
PC141
1000P
PC143
0.1U
PR126
0.02
PR122
0.02
PF2
TR/SFT-10A
PL18
120Z/100M
PL17
120Z/100M
PL16
120Z/100M
PR145
0
PR143
0
PJ2
P24
Battery Connector
+5VAS
PR133
4.7K
PR124
12.1K
PR123
1M
DBATT
PQ40
SCK431LCK-5
PR132
402K
PR127
30.9K
PC136
0.1U
PU21B

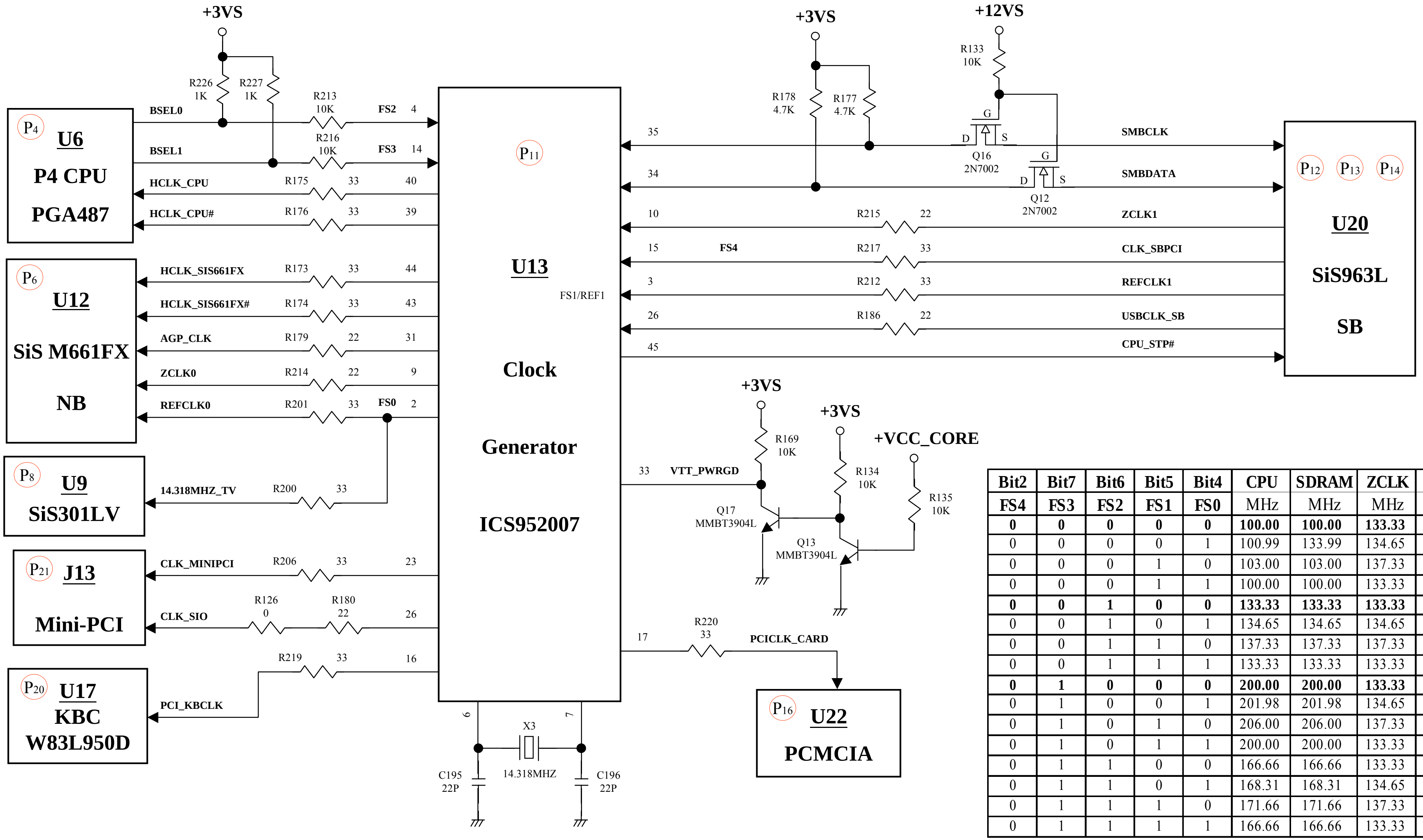
8.3 No Display (1)

There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module,DIMM memory are installed properly.
Display OK?
Yes
Correct it.
No
1. Try another known good CPU module, DIMM module And BIOS.
2. Remove all of I/O device (HDD, CD-ROM…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting
If 378 Port Have error code
Yes
According error Cord to repair
No
Check system clock and reset circuit.
To be continued Clock and reset checking

8.3 No Display (2)

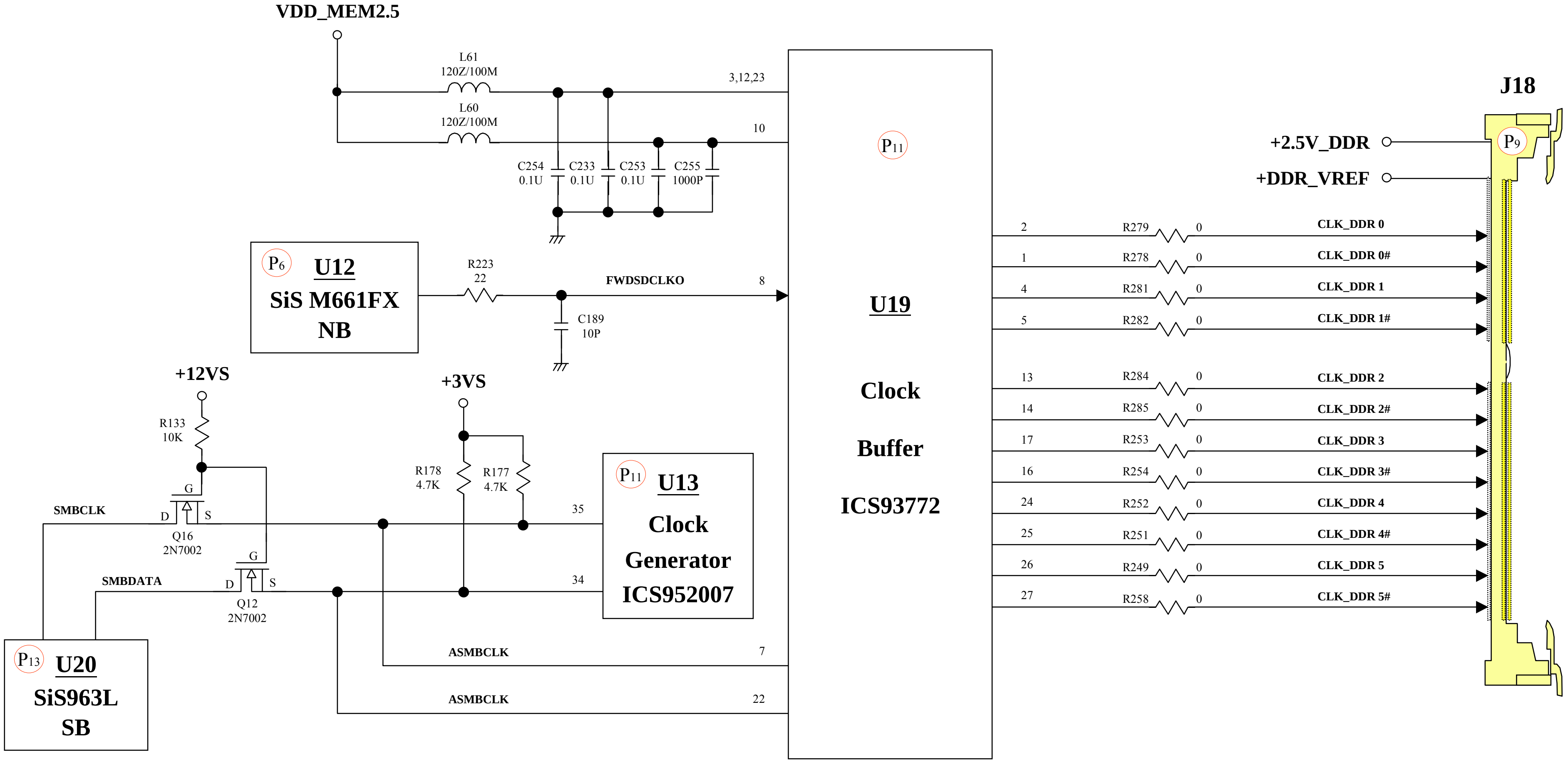
System Clock Check


+3VS
R226
1K
R227
1K
R213
10K
FS2
4
BSEL0
R216
10K
FS3
14
BSEL1
P4
U6
P4 CPU
PGA487
HCLK_CPU
R175
33
40
HCLK_CPU#
R176
33
39
P6
U12
SiS M661FX
NB
HCLK_SIS661FX
R173
33
44
HCLK_SIS661FX#
R174
33
43
AGP_CLK
R179
22
31
ZCLK0
R214
22
9
REFCLK0
R201
33
FS0
2
P8
U9
SiS301LV
14.318MHZ_TV
R200
33
P21
J13
Mini-PCI
CLK_MINIPCI
R206
33
23
CLK_SIO
R126
0
R180
22
26
P20
U17
KBC
W83L950D
PCI_KBCLK
R219
33
16
P11
U13
FS1/REF1
Clock
Generator
ICS952007
6
7
X3
14.318MHZ
C195
22P
C196
22P
+3VS
R178
4.7K
R177
4.7K
+12VS
R133
10K
G
D
S
Q16
2N7002
G
D
S
Q12
2N7002
35
SMBCLK
34
SMBDATA
10
R215
22
ZCLK1
15
FS4
R217
33
CLK_SBPCI
3
R212
33
REFCLK1
26
R186
22
USBCLK_SB
45
CPU_STP#
P12
P13
P14
U20
SiS963L
SB
+3VS
R169
10K
+3VS
R134
10K
+VCC_CORE
R135
10K
33
VTT_PWRGD
Q17
MMBT3904L
Q13
MMBT3904L
17
R220
33
PCICLK_CARD
P16
U22
PCMCIA

Bit2	Bit7	Bit6	Bit5	Bit4	CPU	SDRAM	ZCLK	AGP	PCI
FS4	**FS3**	**FS2**	**FS1**	**FS0**	MHz	MHz	MHz	MHz	MHz
0	**0**	**0**	**0**	**0**	**100.00**	**100.00**	**133.33**	**66.66**	**33.33**
0	0	0	0	1	100.99	133.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	66.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	**0**	**1**	**0**	**0**	**133.33**	**133.33**	**133.33**	**66.66**	**33.33**
0	0	1	0	1	134.65	134.65	134.65	67.32	33.66
0	0	1	1	0	137.33	137.33	137.33	68.66	34.33
0	0	1	1	1	133.33	133.33	133.33	66.67	33.33
0	**1**	**0**	**0**	**0**	**200.00**	**200.00**	**133.33**	**66.67**	**33.33**
0	1	0	0	1	201.98	201.98	134.65	67.33	33.66
0	1	0	1	0	206.00	206.00	137.33	68.67	34.33
0	1	0	1	1	200.00	200.00	133.33	66.67	33.33
0	1	1	0	0	166.66	166.66	133.33	66.66	33.33
0	1	1	0	1	168.31	168.31	134.65	67.32	33.66
0	1	1	1	0	171.66	171.66	137.33	68.66	34.33
0	1	1	1	1	166.66	166.66	133.33	66.66	33.33

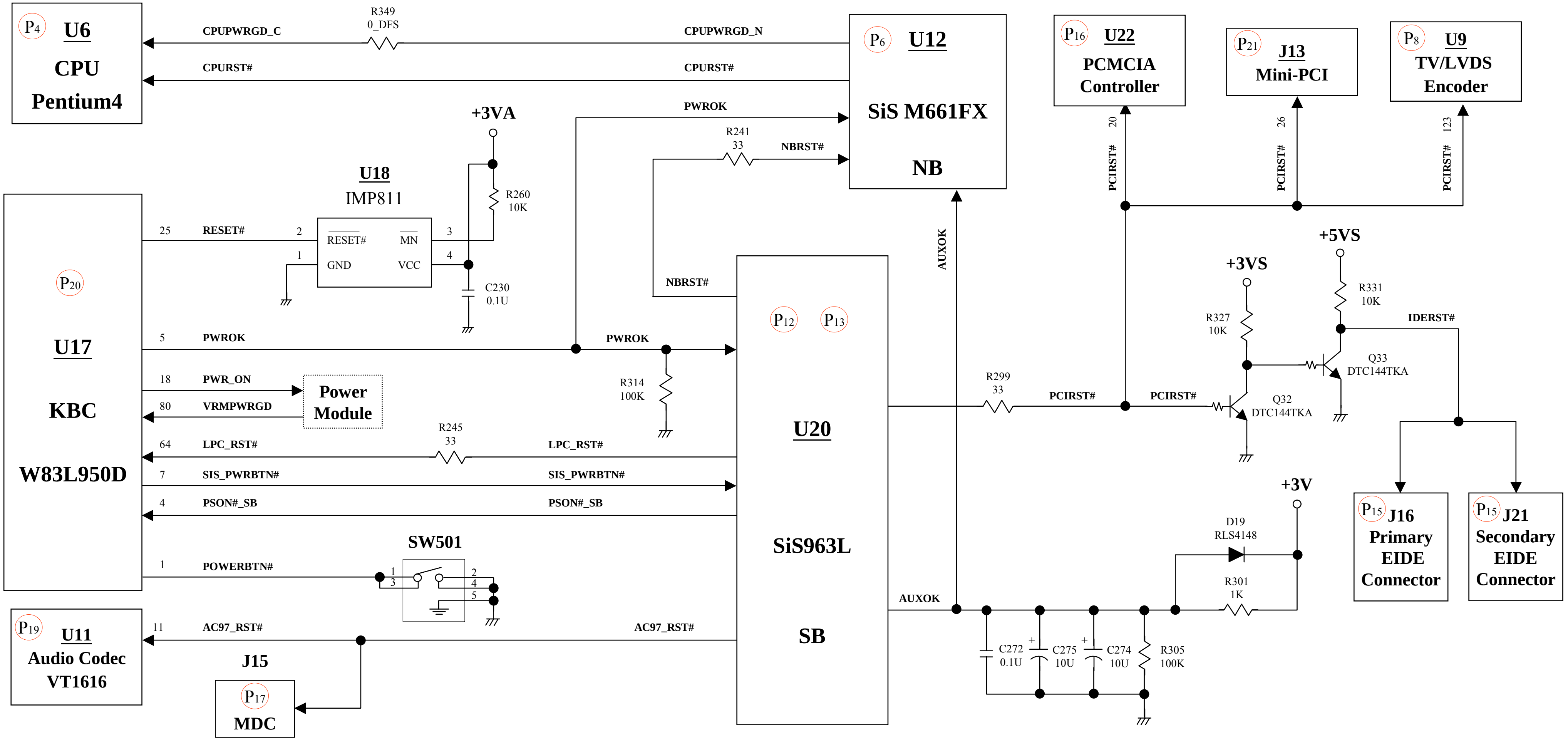
8.3 No Display (3)

DDR Clock Check


VDD_MEM2.5
L61
120Z/100M
L60
120Z/100M
3,12,23
10
C254
0.1U
C233
0.1U
C253
0.1U
C255
1000P
P11
U19
Clock
Buffer
ICS93772
J18
P9
+2.5V_DDR
+DDR_VREF
P6
U12
SiS M661FX
NB
R223
22
FWDSDCLKO
8
C189
10P
2 R279 0 CLK_DDR 0
1 R278 0 CLK_DDR 0#
4 R281 0 CLK_DDR 1
5 R282 0 CLK_DDR 1#
13 R284 0 CLK_DDR 2
14 R285 0 CLK_DDR 2#
17 R253 0 CLK_DDR 3
16 R254 0 CLK_DDR 3#
24 R252 0 CLK_DDR 4
25 R251 0 CLK_DDR 4#
26 R249 0 CLK_DDR 5
27 R258 0 CLK_DDR 5#
+12VS
R133
10K
+3VS
R178
4.7K
R177
4.7K
P11
U13
Clock
Generator
ICS952007
35
34
SMBCLK
G
D
S
Q16
2N7002
SMBDATA
G
D
S
Q12
2N7002
ASMBCLK
7
ASMBCLK
22
P13
U20
SiS963L
SB

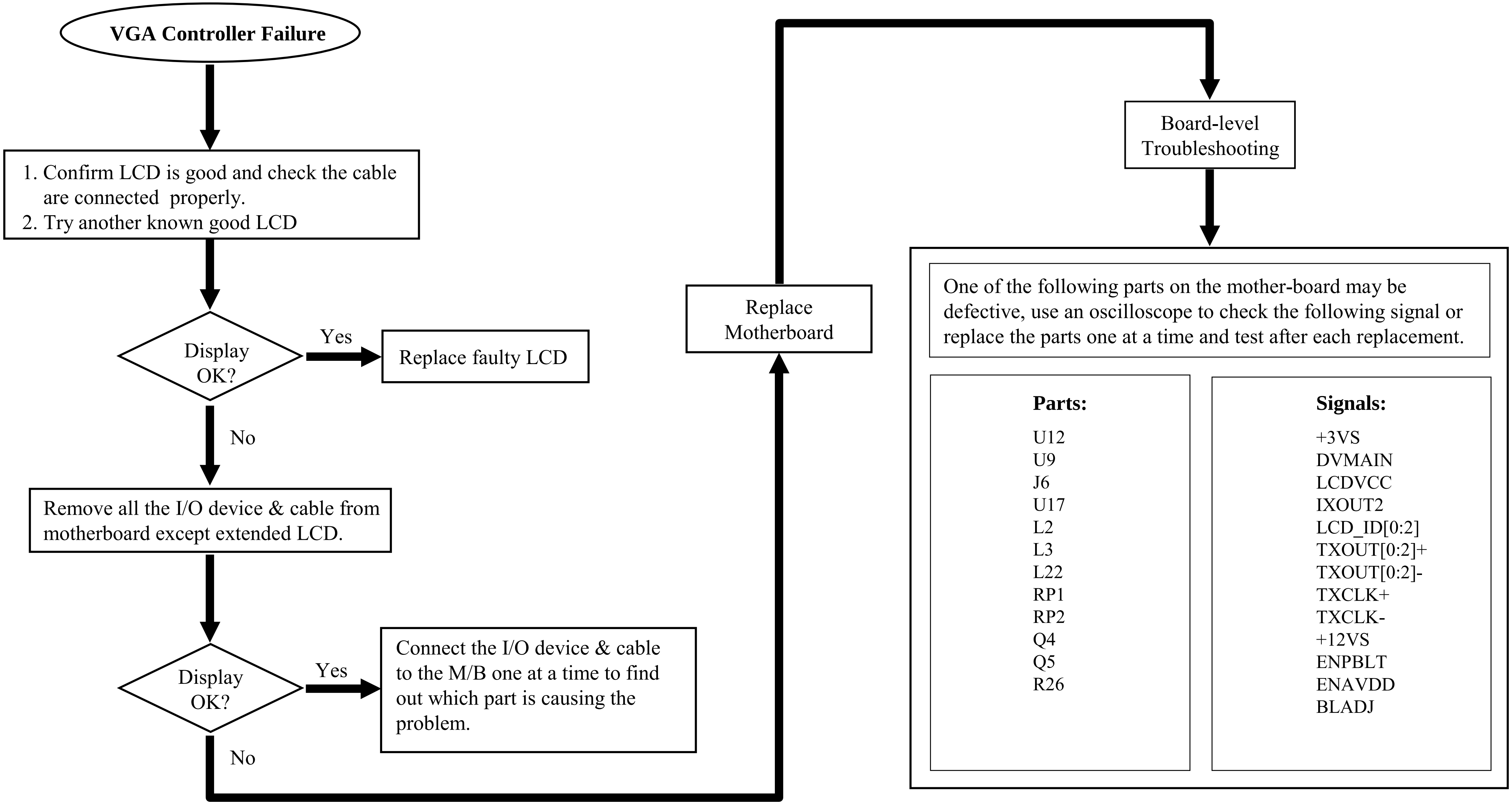
8.3 No Display (4)

System Reset Check


P4
U6
CPU
Pentium4
CPUPWRGD_C
R349
0_DFS
CPUPWRGD_N
CPURST#
CPURST#
P6
U12
SiS M661FX
NB
PWROK
R241
33
NBRST#
+3VA
U18
IMP811
R260
10K
RESET#
MN
GND
VCC
C230
0.1U
P16
U22
PCMCIA
Controller
P21
J13
Mini-PCI
P8
U9
TV/LVDS
Encoder
20
26
123
PCIRST#
PCIRST#
PCIRST#
AUXOK
P20
U17
KBC
W83L950D
25
RESET#
2
1
3
4
5
PWROK
18
PWR_ON
80
VRMPWRGD
Power
Module
R314
100K
64
LPC_RST#
R245
33
LPC_RST#
7
SIS_PWRBTN#
SIS_PWRBTN#
4
PSON#_SB
PSON#_SB
NBRST#
P12
P13
U20
SiS963L
SB
R299
33
PCIRST#
PCIRST#
+3VS
R327
10K
Q32
DTC144TKA
+5VS
R331
10K
IDERST#
Q33
DTC144TKA
P15
J16
Primary
EIDE
Connector
P15
J21
Secondary
EIDE
Connector
+3V
D19
RLS4148
R301
1K
AUXOK
C272
0.1U
C275
10U
C274
10U
R305
100K
SW501
1
POWERBTN#
1
3
2
4
5
P19
U11
Audio Codec
VT1616
11
AC97_RST#
AC97_RST#
J15
P17
MDC

8.4 LCD No Display or Picture Abnormal (1)

There is no display or picture abnormal on LCD or monitor.


VGA Controller Failure
Display OK?
Yes
No
Replace faulty LCD
Display OK?
Yes
No
Replace Motherboard
Board-level Troubleshooting

1. Confirm LCD is good and check the cable are connected properly.
2. Try another known good LCD

Remove all the I/O device & cable from motherboard except extended LCD.

Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

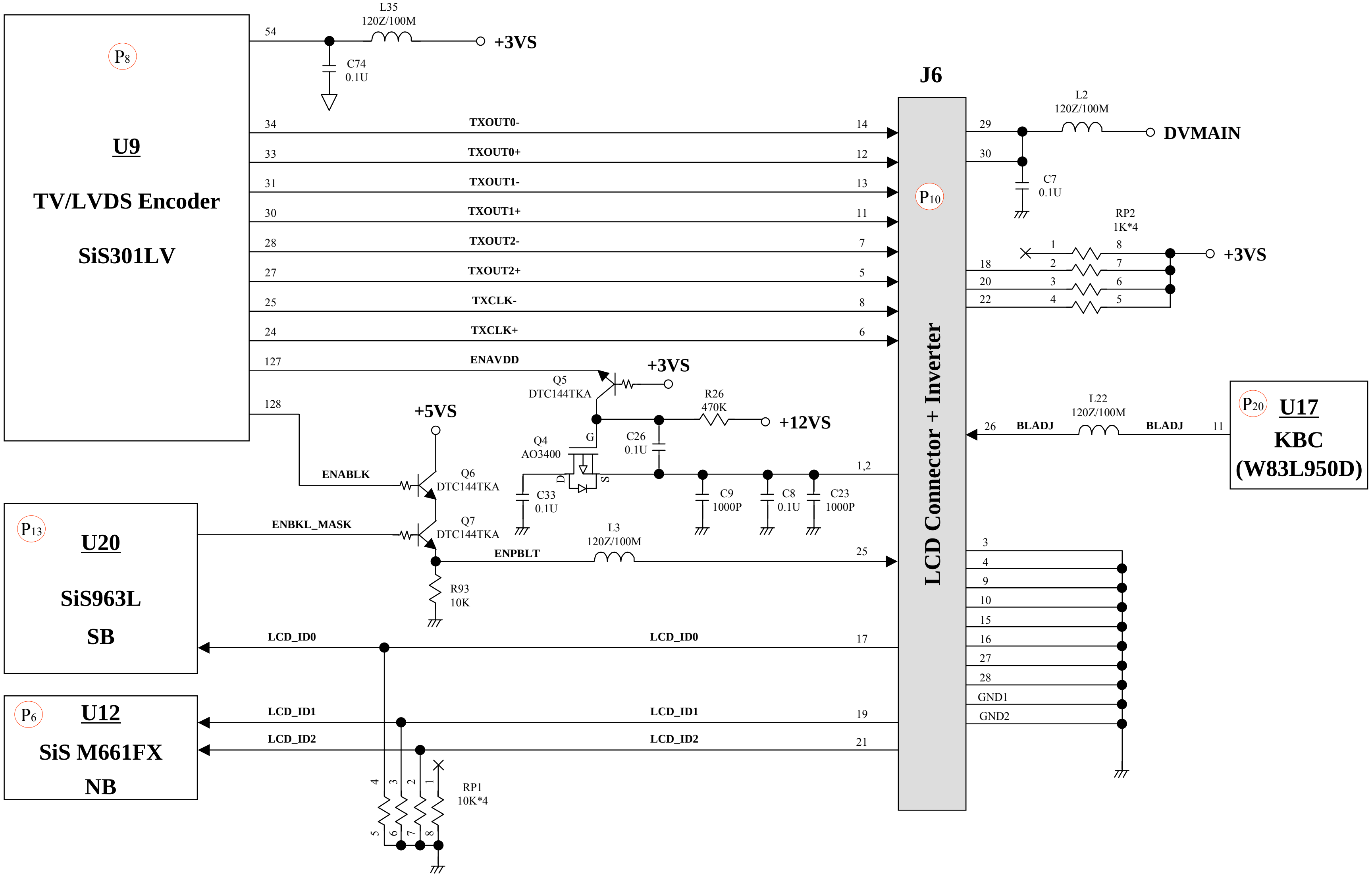
U12
U9
J6
U17
L2
L3
L22
RP1
RP2
Q4
Q5
R26

Signals:

+3VS
DVMAIN
LCDVCC
IXOUT2
LCD_ID[0:2]
TXOUT[0:2]+
TXOUT[0:2]-
TXCLK+
TXCLK-
+12VS
ENPBLT
ENAVDD
BLADJ

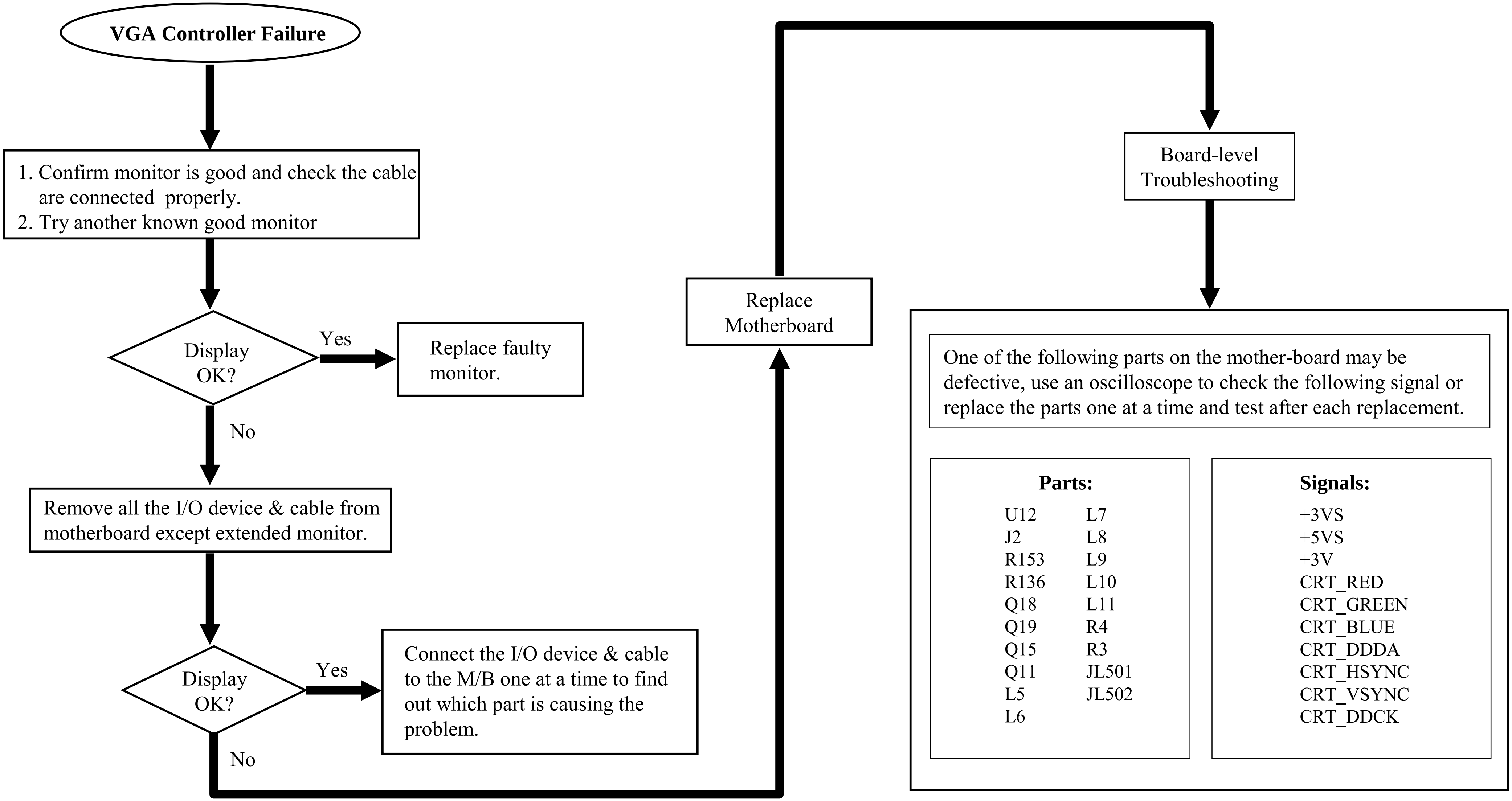
8.4 LCD No Display or Picture Abnormal (2)

There is no display or picture abnormal on LCD or monitor.


P8
U9
TV/LVDS Encoder
SiS301LV
54
L35
120Z/100M
+3VS
C74
0.1U
J6
34 TXOUT0- 14
33 TXOUT0+ 12
31 TXOUT1- 13
30 TXOUT1+ 11
28 TXOUT2- 7
27 TXOUT2+ 5
25 TXCLK- 8
24 TXCLK+ 6
127 ENAVDD
128
Q5
DTC144TKA
+3VS
R26
470K
+12VS
+5VS
Q4
AO3400
G
D
S
C26
0.1U
C33
0.1U
1,2
C9
1000P
C8
0.1U
C23
1000P
ENABLK
Q6
DTC144TKA
ENBKL_MASK
Q7
DTC144TKA
L3
120Z/100M
ENPBLT
25
R93
10K
P13
U20
SiS963L
SB
LCD_ID0
LCD_ID0
17
P6
U12
SiS M661FX
NB
LCD_ID1
LCD_ID1
19
LCD_ID2
LCD_ID2
21
RP1
10K*4
1 2 3 4
5 6 7 8
P10
LCD Connector + Inverter
L2
120Z/100M
29
30
DVMAIN
C7
0.1U
RP2
1K*4
1 8
18 2 7
20 3 6
22 4 5
+3VS
L22
120Z/100M
26 BLADJ
BLADJ 11
P20
U17
KBC
(W83L950D)
3
4
9
10
15
16
27
28
GND1
GND2

8.5 External Monitor No Display or Color Abnormal (1)

There is no display or picture abnormal on monitor.


VGA Controller Failure
Display OK?
Yes
No
Replace faulty monitor.
Display OK?
Yes
No
Replace Motherboard
Board-level Troubleshooting

1. Confirm monitor is good and check the cable are connected properly.
2. Try another known good monitor

Remove all the I/O device & cable from motherboard except extended monitor.

Connect the I/O device & cable to the M/B one at a time to find out which part is causing the problem.

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

U12
J2
R153
R136
Q18
Q19
Q15
Q11
L5
L6
L7
L8
L9
L10
L11
R4
R3
JL501
JL502

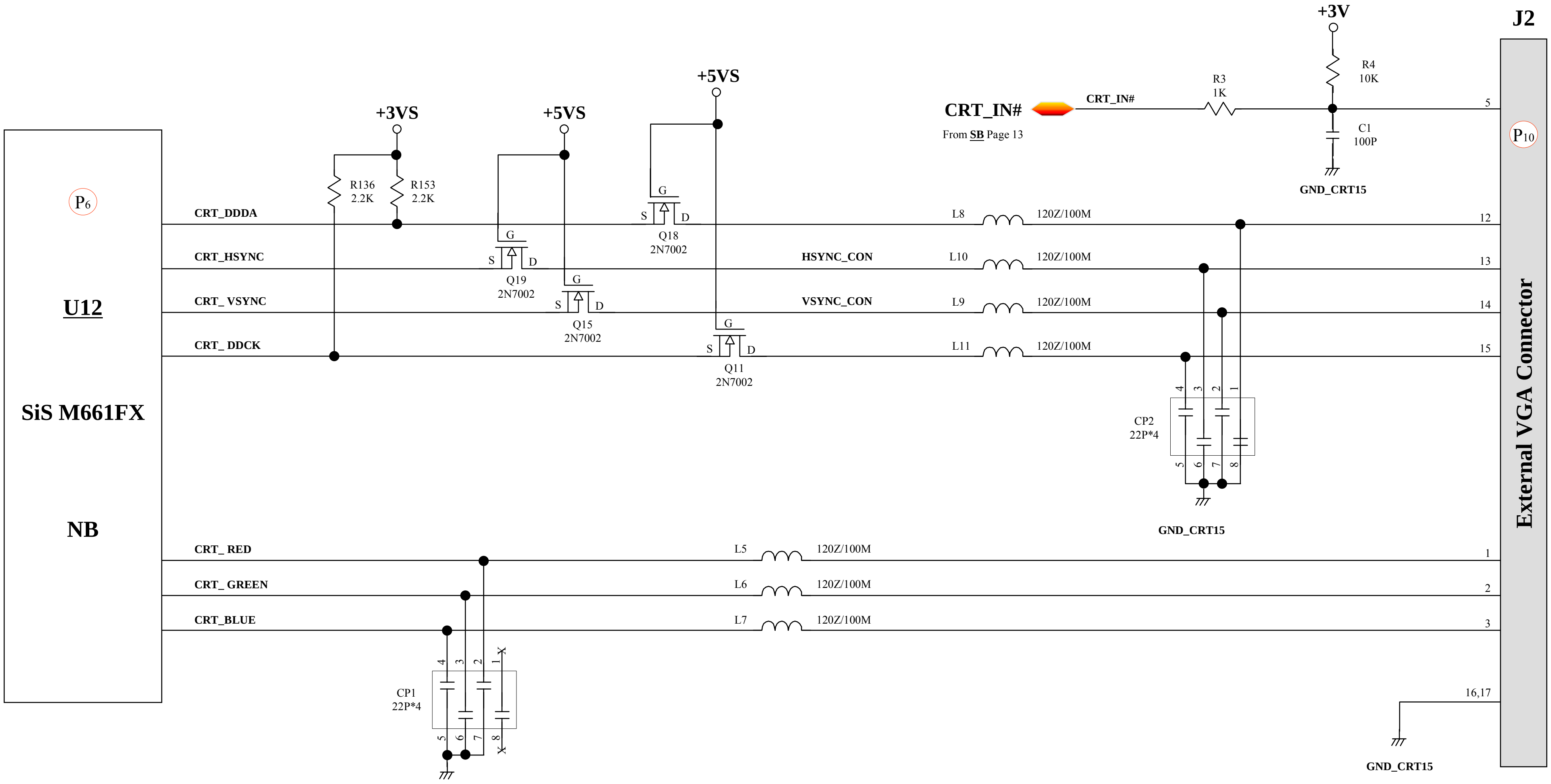
Signals:

+3VS
+5VS
+3V
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_DDDA
CRT_HSYNC
CRT_VSYNC
CRT_DDCK

8599 N/B Maintenance

8.5 External Monitor No Display or Color Abnormal (2)

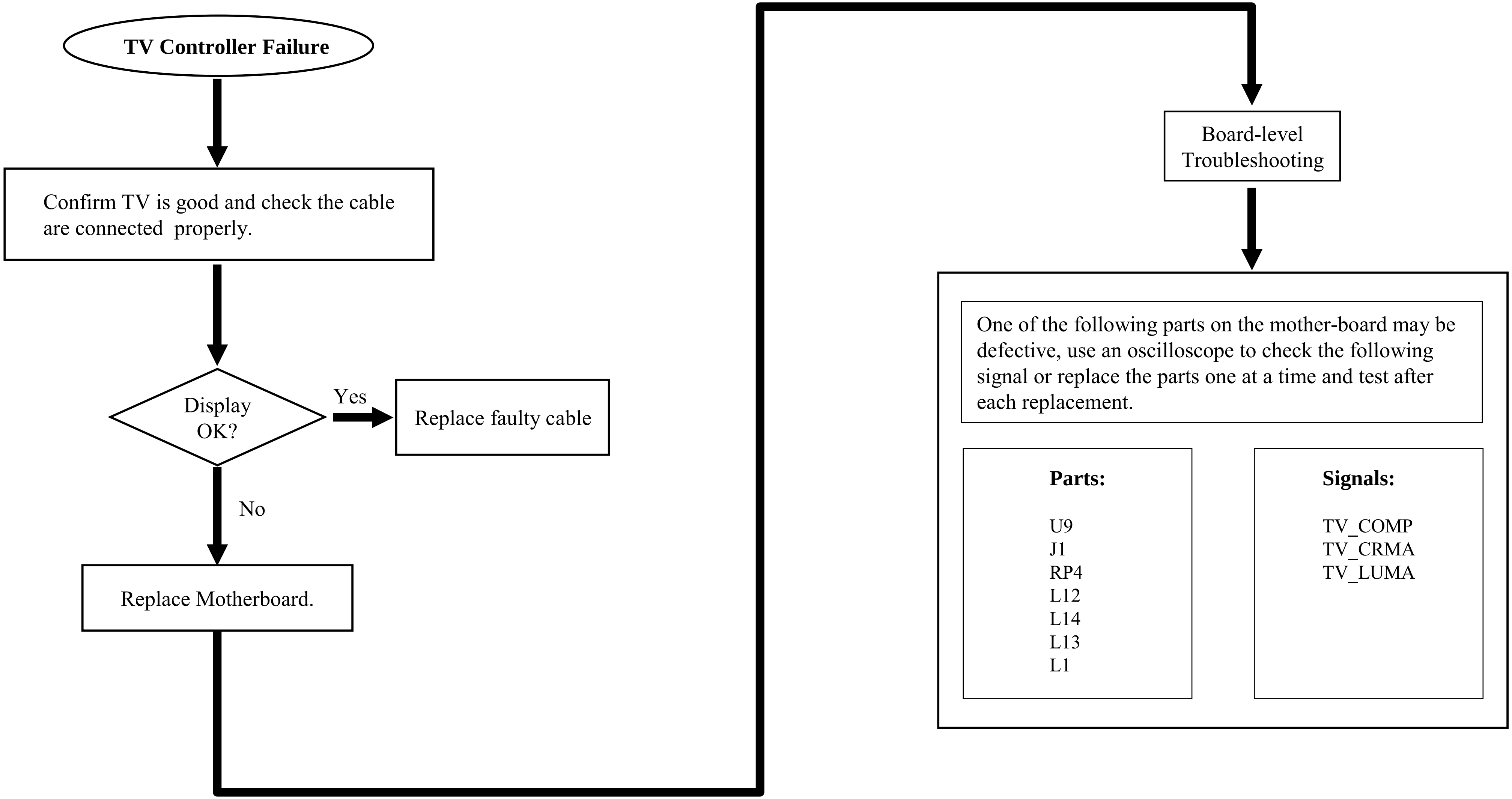
There is no display or picture abnormal on monitor.



+3V
J2
R4
10K
R3
1K
CRT_IN#
+5VS
CRT_IN#
From SB Page 13
C1
100P
P10
GND_CRT15
+3VS
+5VS
R136
2.2K
R153
2.2K
P6
CRT_DDDA
CRT_HSYNC
CRT_ VSYNC
CRT_ DDCK
U12
SiS M661FX
NB
G
S
D
Q18
2N7002
Q19
2N7002
Q15
2N7002
Q11
2N7002
HSYNC_CON
VSYNC_CON
L8
L10
L9
L11
120Z/100M
12
13
14
15
5
CP2
22P*4
GND_CRT15
External VGA Connector
CRT_ RED
CRT_ GREEN
CRT_BLUE
L5
L6
L7
1
2
3
CP1
22P*4
16,17
GND_CRT15

8.6 TV Test Error (1)

There is no display or picture abnormal on TV.


TV Controller Failure
Confirm TV is good and check the cable are connected properly.
Display OK?
Yes
Replace faulty cable
No
Replace Motherboard.
Board-level Troubleshooting

One of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

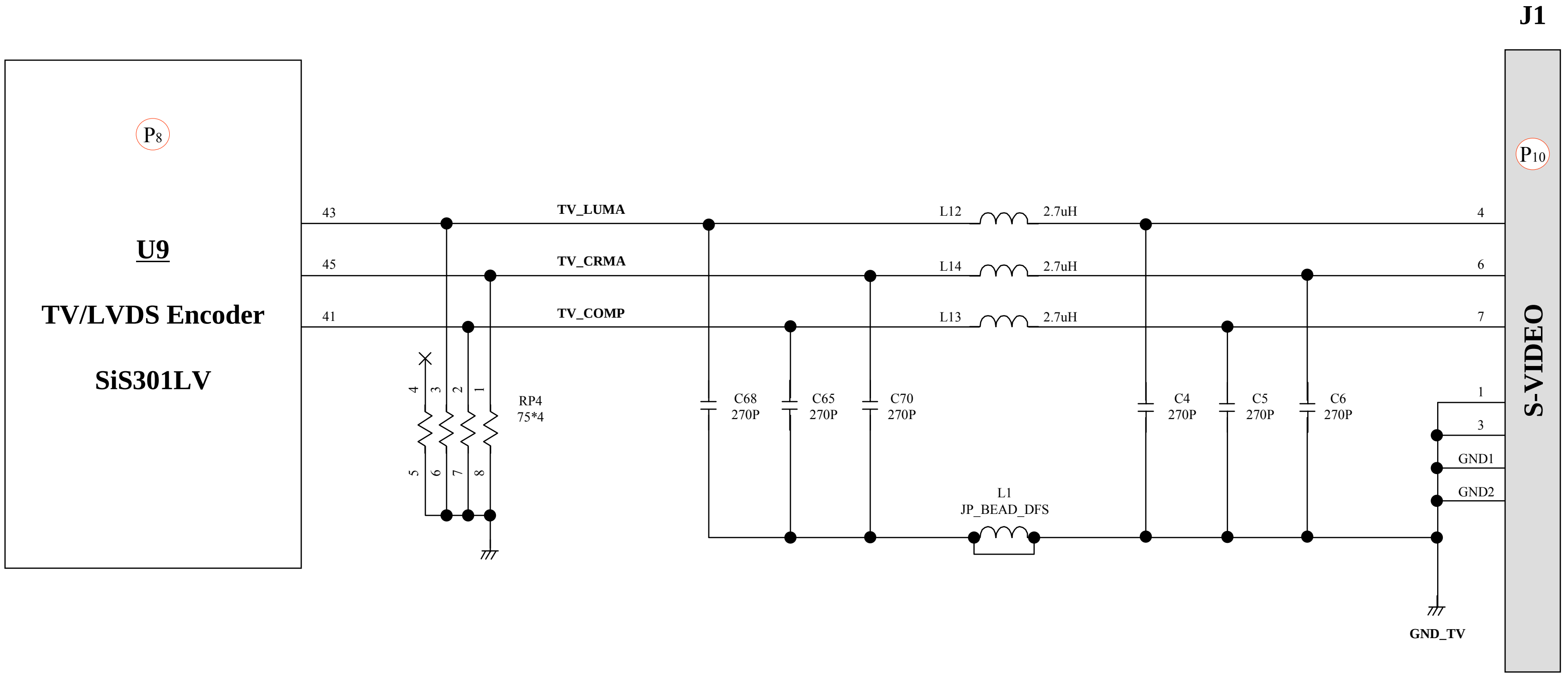
- U9
- J1
- RP4
- L12
- L14
- L13
- L1

Signals:

- TV_COMP
- TV_CRMA
- TV_LUMA

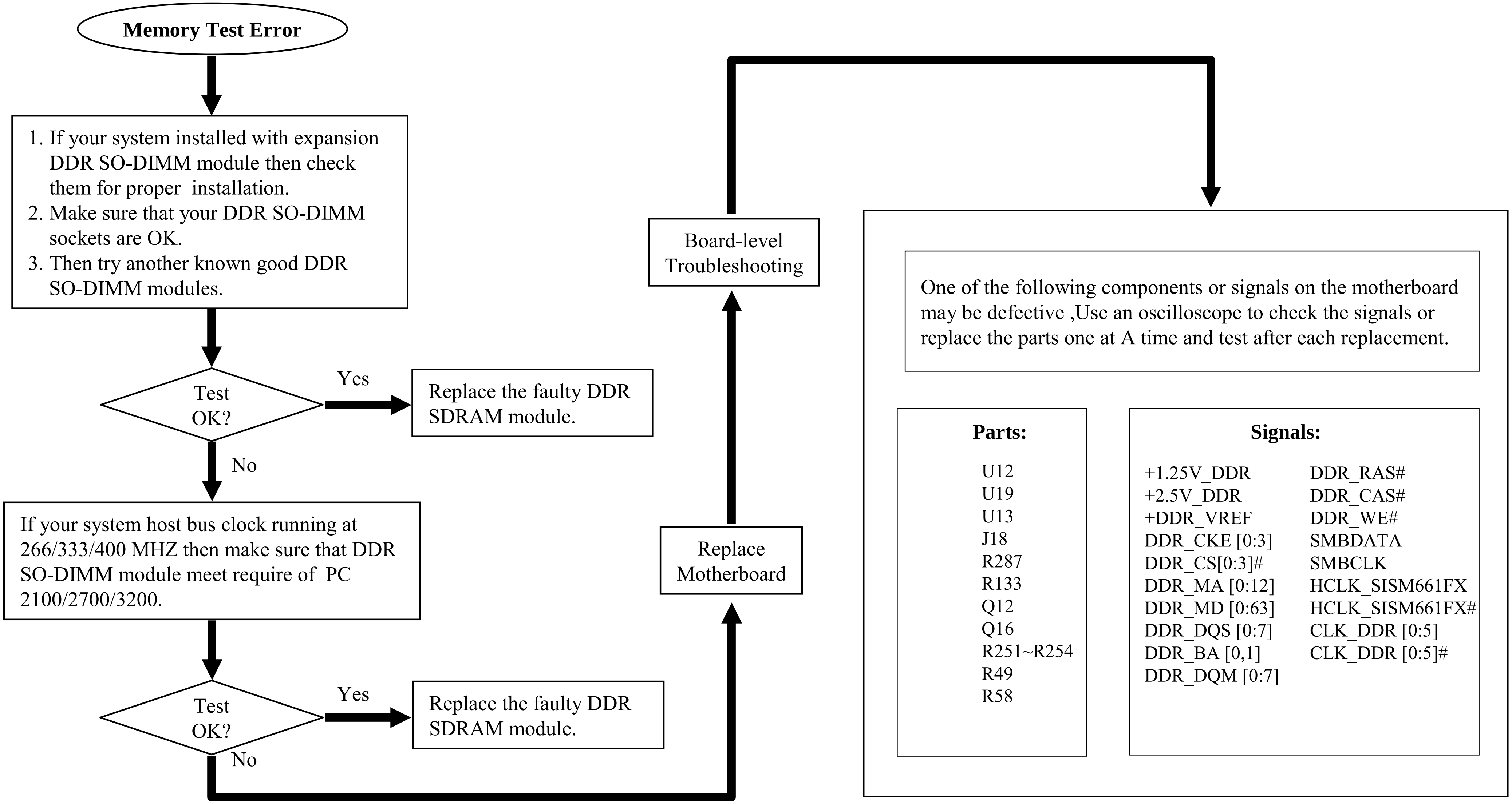
8.6 TV Test Error (2)

There is no display or picture abnormal on TV.


J1
P8
U9
TV/LVDS Encoder
SiS301LV
P10
43
45
41
TV_LUMA
TV_CRMA
TV_COMP
RP4
75*4
4
3
2
1
5
6
7
8
C68
270P
C65
270P
C70
270P
L12
2.7uH
L14
2.7uH
L13
2.7uH
L1
JP_BEAD_DFS
C4
270P
C5
270P
C6
270P
4
6
7
1
3
GND1
GND2
GND_TV
S-VIDEO

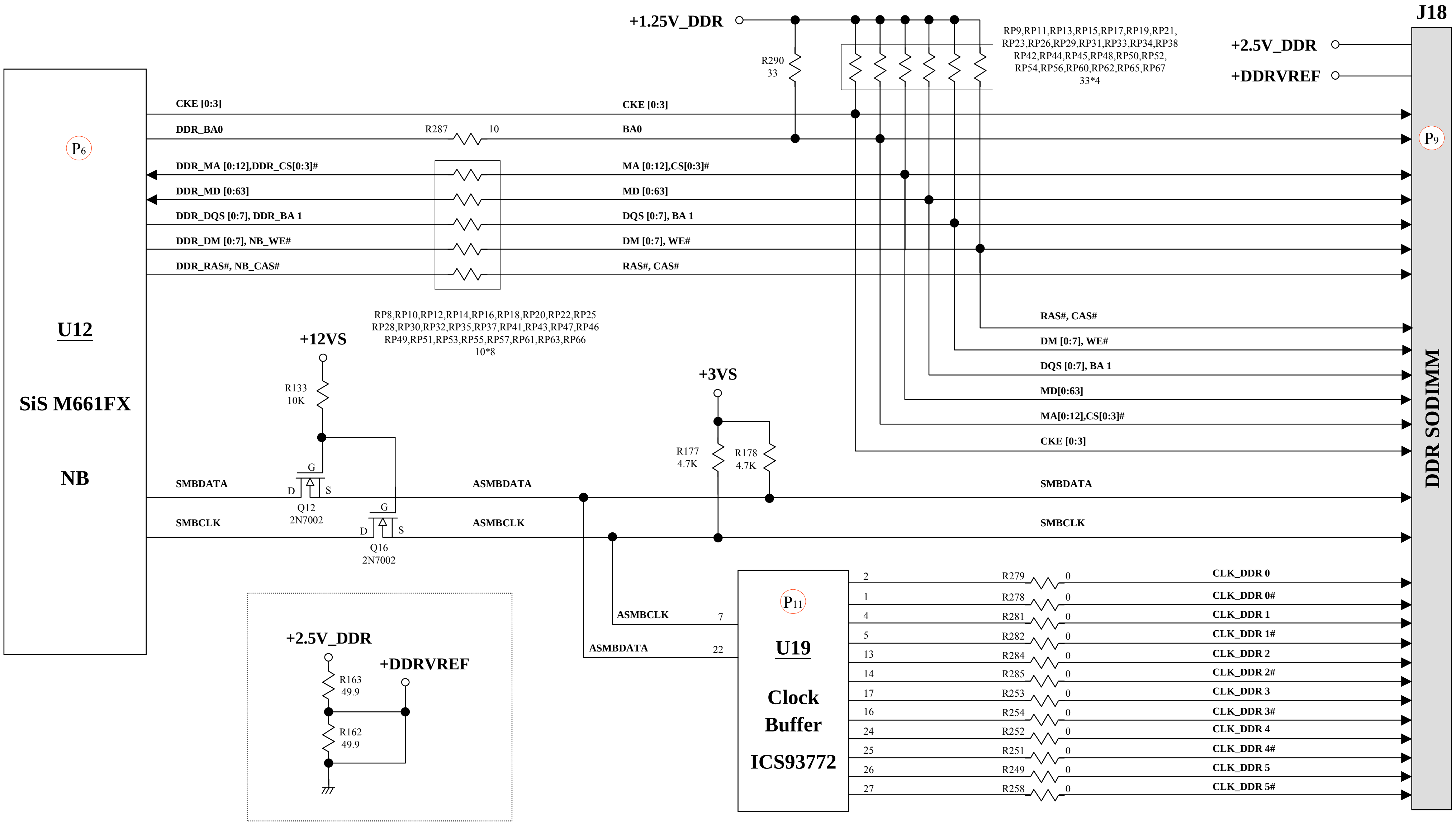
8.7 Memory Test Error (1)

Extend DDRAM is failure or system hangs up.


Memory Test Error
1. If your system installed with expansion DDR SO-DIMM module then check them for proper installation.
2. Make sure that your DDR SO-DIMM sockets are OK.
3. Then try another known good DDR SO-DIMM modules.
Test OK?
Yes
Replace the faulty DDR SDRAM module.
No
If your system host bus clock running at 266/333/400 MHZ then make sure that DDR SO-DIMM module meet require of PC 2100/2700/3200.
Test OK?
Yes
Replace the faulty DDR SDRAM module.
No
Replace Motherboard
Board-level Troubleshooting
One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.
Parts:
U12
U19
U13
J18
R287
R133
Q12
Q16
R251~R254
R49
R58
Signals:
+1.25V_DDR
+2.5V_DDR
+DDR_VREF
DDR_CKE [0:3]
DDR_CS[0:3]#
DDR_MA [0:12]
DDR_MD [0:63]
DDR_DQS [0:7]
DDR_BA [0,1]
DDR_DQM [0:7]
DDR_RAS#
DDR_CAS#
DDR_WE#
SMBDATA
SMBCLK
HCLK_SISM661FX
HCLK_SISM661FX#
CLK_DDR [0:5]
CLK_DDR [0:5]#

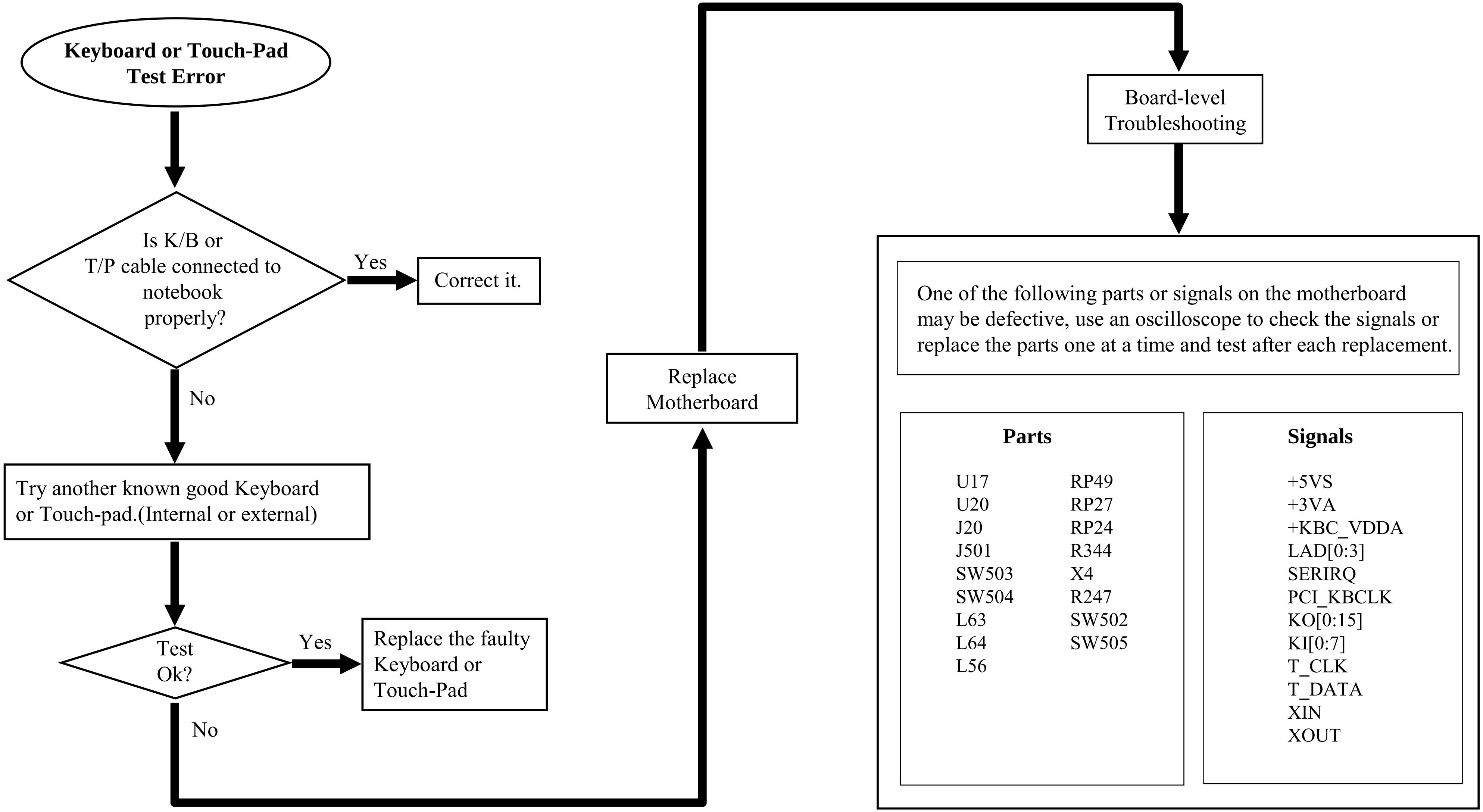
8.7 Memory Test Error (2)

Extend DDRAM is failure or system hangs up.


+1.25V_DDR
J18
R290
33
RP9,RP11,RP13,RP15,RP17,RP19,RP21,
RP23,RP26,RP29,RP31,RP33,RP34,RP38
RP42,RP44,RP45,RP48,RP50,RP52,
RP54,RP56,RP60,RP62,RP65,RP67
33*4
+2.5V_DDR
+DDRVREF
CKE [0:3]
DDR_BA0
R287
10
BA0
P6
P9
DDR_MA [0:12],DDR_CS[0:3]#
MA [0:12],CS[0:3]#
DDR_MD [0:63]
MD [0:63]
DDR_DQS [0:7], DDR_BA 1
DQS [0:7], BA 1
DDR_DM [0:7], NB_WE#
DM [0:7], WE#
DDR_RAS#, NB_CAS#
RAS#, CAS#
U12
SiS M661FX
NB
RP8,RP10,RP12,RP14,RP16,RP18,RP20,RP22,RP25
RP28,RP30,RP32,RP35,RP37,RP41,RP43,RP47,RP46
RP49,RP51,RP53,RP55,RP57,RP61,RP63,RP66
10*8
+12VS
R133
10K
+3VS
RAS#, CAS#
DM [0:7], WE#
DQS [0:7], BA 1
MD[0:63]
MA[0:12],CS[0:3]#
CKE [0:3]
DDR SODIMM
R177
4.7K
R178
4.7K
SMBDATA
G
D
S
Q12
2N7002
ASMBDATA
SMBDATA
SMBCLK
Q16
2N7002
ASMBCLK
SMBCLK
+2.5V_DDR
+DDRVREF
R163
49.9
R162
49.9
ASMBCLK
7
ASMBDATA
22
P11
U19
Clock
Buffer
ICS93772
2 R279 0 CLK_DDR 0
1 R278 0 CLK_DDR 0#
4 R281 0 CLK_DDR 1
5 R282 0 CLK_DDR 1#
13 R284 0 CLK_DDR 2
14 R285 0 CLK_DDR 2#
17 R253 0 CLK_DDR 3
16 R254 0 CLK_DDR 3#
24 R252 0 CLK_DDR 4
25 R251 0 CLK_DDR 4#
26 R249 0 CLK_DDR 5
27 R258 0 CLK_DDR 5#

8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

Error message of keyboard or touch-pad failure is shown or any key does not work.


Keyboard or Touch-Pad Test Error
Is K/B or T/P cable connected to notebook properly?
Yes
Correct it.
No
Try another known good Keyboard or Touch-pad.(Internal or external)
Test Ok?
Yes
Replace the faulty Keyboard or Touch-Pad
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts

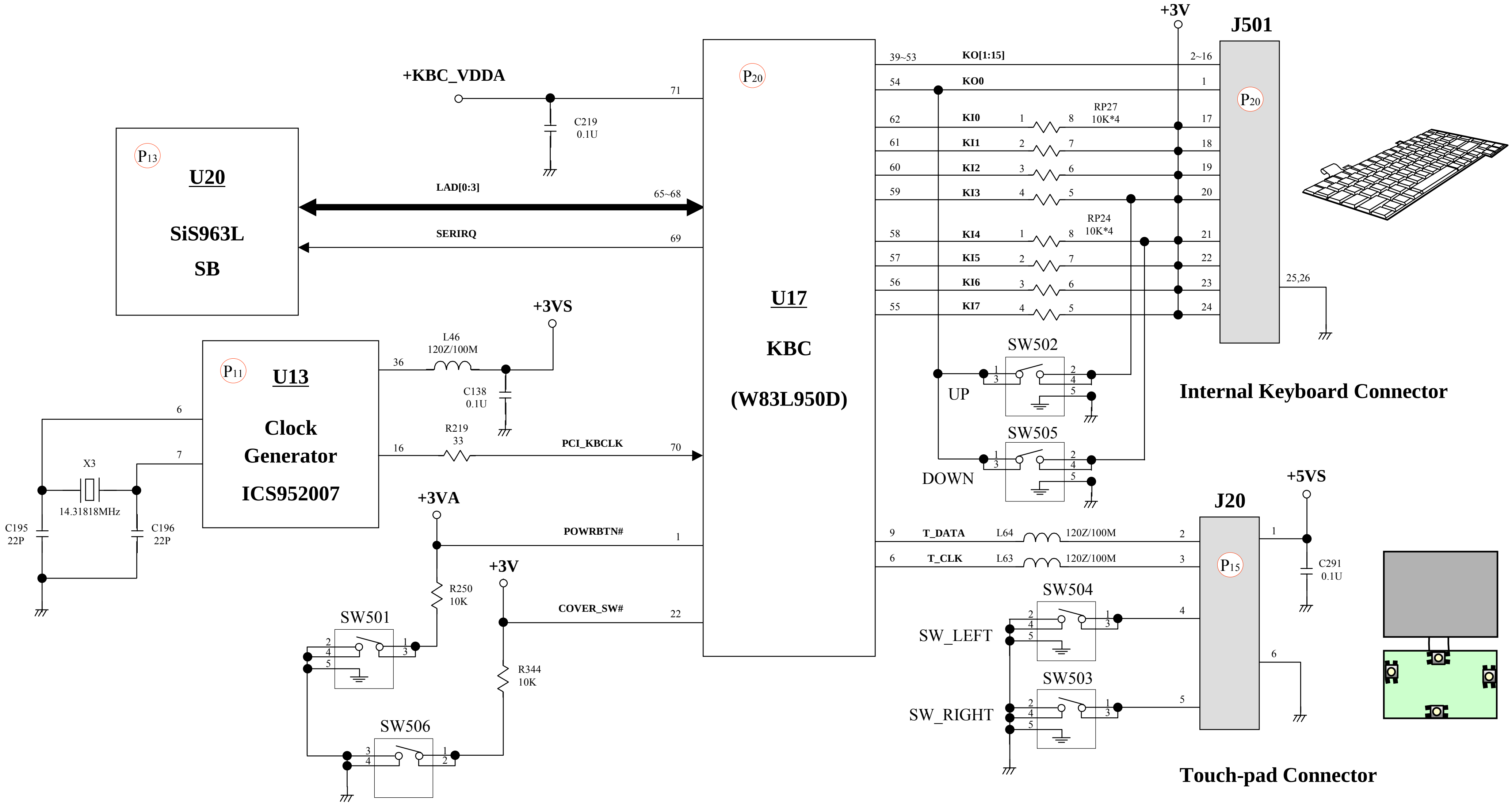
- U17
- U20
- J20
- J501
- SW503
- SW504
- L63
- L64
- L56
- RP49
- RP27
- RP24
- R344
- X4
- R247
- SW502
- SW505

Signals

- +5VS
- +3VA
- +KBC_VDDA
- LAD[0:3]
- SERIRQ
- PCI_KBCLK
- KO[0:15]
- KI[0:7]
- T_CLK
- T_DATA
- XIN
- XOUT

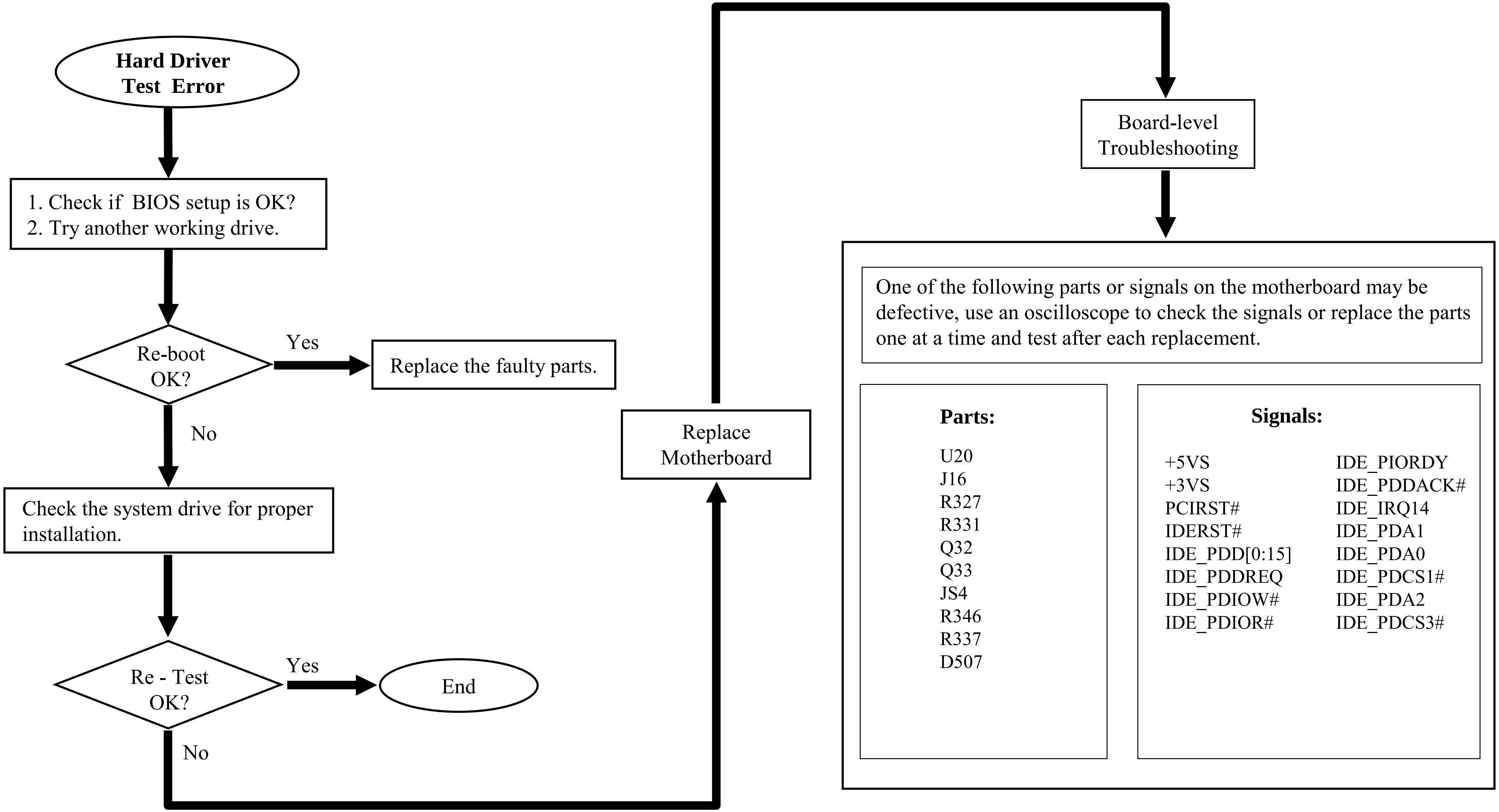
8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

Error message of keyboard or touch-pad failure is shown or any key does not work.


+KBC_VDDA
71
C219
0.1U
P13
U20
SiS963L
SB
LAD[0:3]
65~68
SERIRQ
69
+3VS
L46
120Z/100M
36
C138
0.1U
P11
U13
Clock
Generator
ICS952007
6
7
X3
14.31818MHz
C195
22P
C196
22P
R219
33
16
PCI_KBCLK
70
+3VA
POWRBTN#
1
R250
10K
+3V
COVER_SW#
22
R344
10K
SW501
SW506
P20
U17
KBC
(W83L950D)
39~53
KO[1:15]
54
KO0
62
KI0
61
KI1
60
KI2
59
KI3
58
KI4
57
KI5
56
KI6
55
KI7
RP27
10K*4
RP24
10K*4
+3V
J501
2~16
1
17
18
19
20
21
22
23
24
25,26
P20
SW502
UP
SW505
DOWN
Internal Keyboard Connector
9
T_DATA
L64
120Z/100M
6
T_CLK
L63
120Z/100M
+5VS
J20
P15
C291
0.1U
SW504
SW_LEFT
SW503
SW_RIGHT
Touch-pad Connector

8.9 Hard Drive Test Error (1)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.


Hard Driver Test Error
1. Check if BIOS setup is OK?
2. Try another working drive.
Re-boot OK?
Yes
Replace the faulty parts.
No
Check the system drive for proper installation.
Re - Test OK?
Yes
End
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:

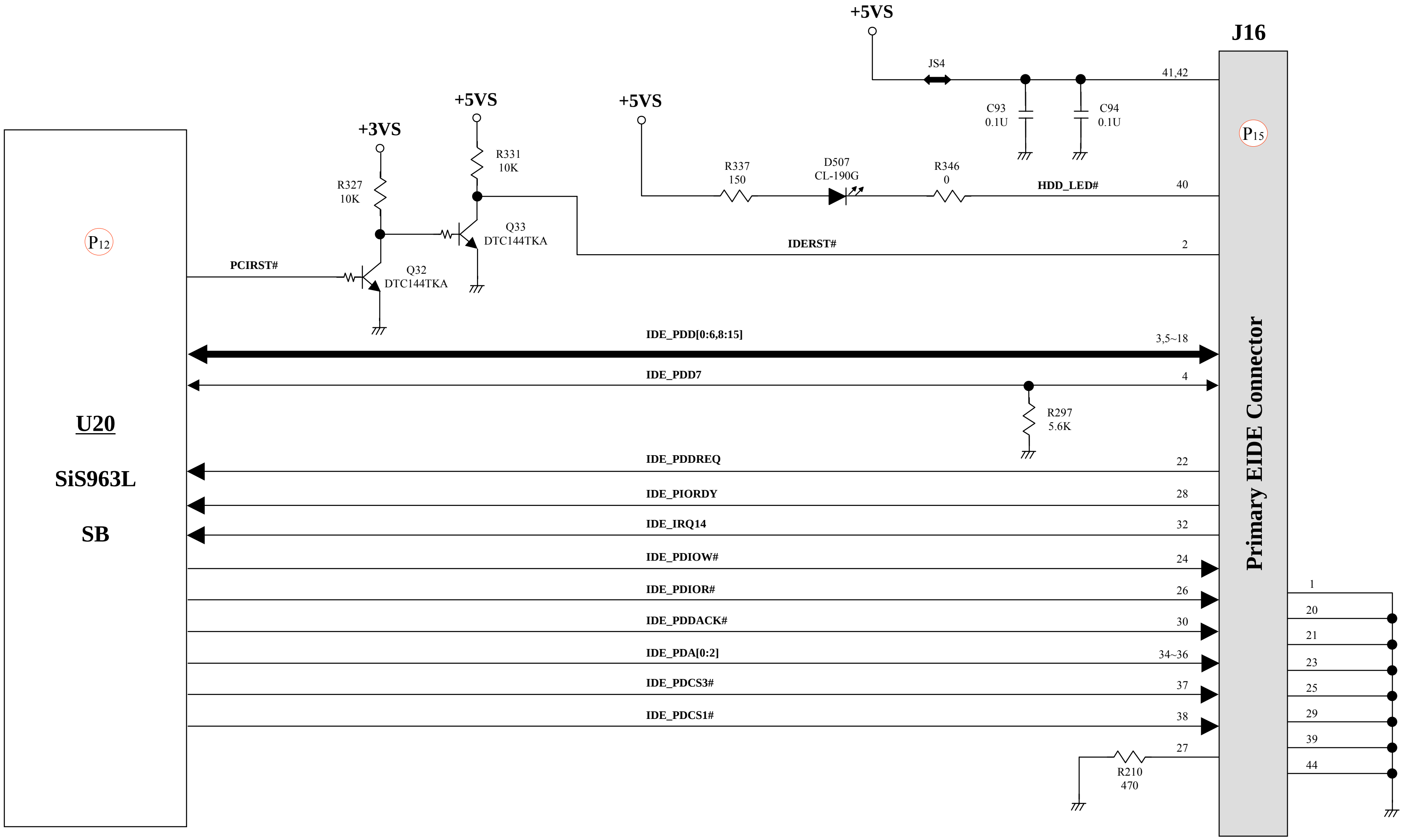
U20
J16
R327
R331
Q32
Q33
JS4
R346
R337
D507

Signals:

+5VS
+3VS
PCIRST#
IDERST#
IDE_PDD[0:15]
IDE_PDDREQ
IDE_PDIOW#
IDE_PDIOR#
IDE_PIORDY
IDE_PDDACK#
IDE_IRQ14
IDE_PDA1
IDE_PDA0
IDE_PDCS1#
IDE_PDA2
IDE_PDCS3#

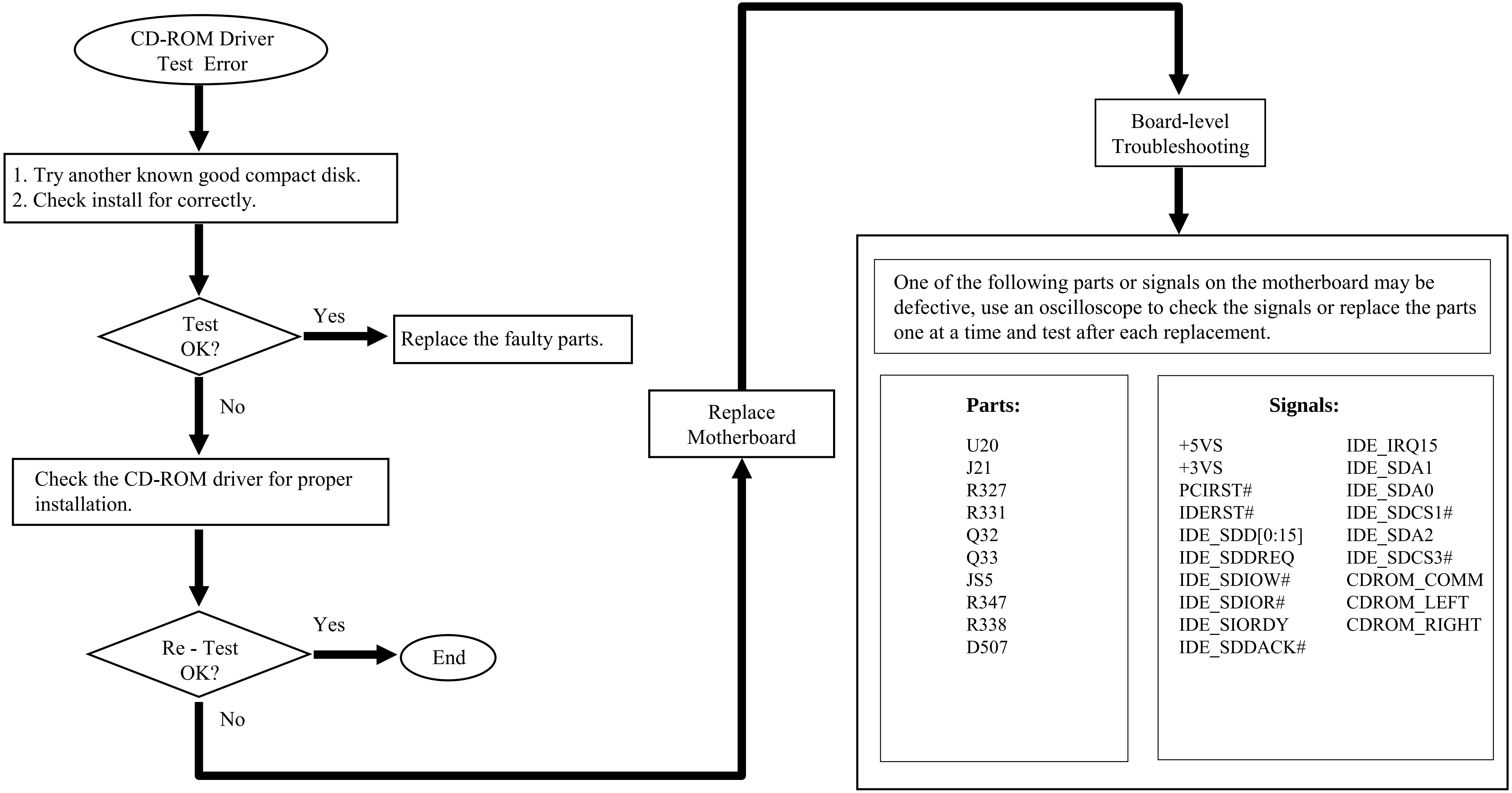
8.9 Hard Drive Test Error (2)

Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.


+5VS
J16
JS4
41,42
C93
0.1U
C94
0.1U
P15
+5VS
+5VS
+3VS
R331
10K
R327
10K
R337
150
D507
CL-190G
R346
0
HDD_LED#
40
Q33
DTC144TKA
IDERST#
2
P12
PCIRST#
Q32
DTC144TKA
IDE_PDD[0:6,8:15]
3,5~18
IDE_PDD7
4
R297
5.6K
U20
SiS963L
SB
IDE_PDDREQ
22
IDE_PIORDY
28
IDE_IRQ14
32
IDE_PDIOW#
24
IDE_PDIOR#
26
IDE_PDDACK#
30
IDE_PDA[0:2]
34~36
IDE_PDCS3#
37
IDE_PDCS1#
38
27
R210
470
Primary EIDE Connector
1
20
21
23
25
29
39
44

8.10 CD-ROM Drive Test Error (1)

An error message is shown when reading data from CD-ROM drive.


CD-ROM Driver Test Error
1. Try another known good compact disk.
2. Check install for correctly.
Test OK?
Yes
Replace the faulty parts.
No
Check the CD-ROM driver for proper installation.
Re - Test OK?
Yes
End
No
Replace Motherboard
Board-level Troubleshooting

One of the following parts or signals on the motherboard may be defective, use an oscilloscope to check the signals or replace the parts one at a time and test after each replacement.

Parts:

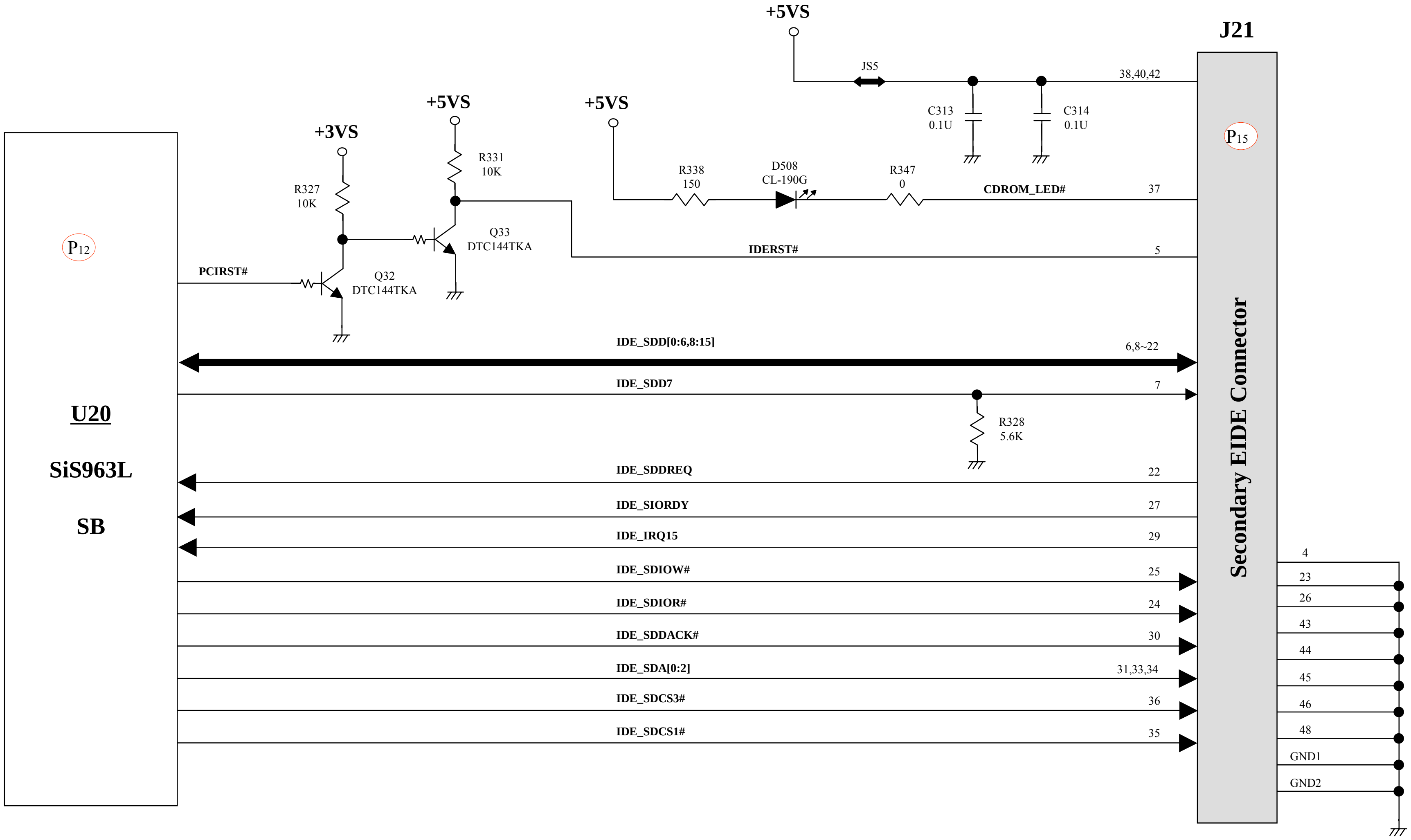
U20
J21
R327
R331
Q32
Q33
JS5
R347
R338
D507

Signals:

+5VS
+3VS
PCIRST#
IDERST#
IDE_SDD[0:15]
IDE_SDDREQ
IDE_SDIOW#
IDE_SDIOR#
IDE_SIORDY
IDE_SDDACK#
IDE_IRQ15
IDE_SDA1
IDE_SDA0
IDE_SDCS1#
IDE_SDA2
IDE_SDCS3#
CDROM_COMM
CDROM_LEFT
CDROM_RIGHT

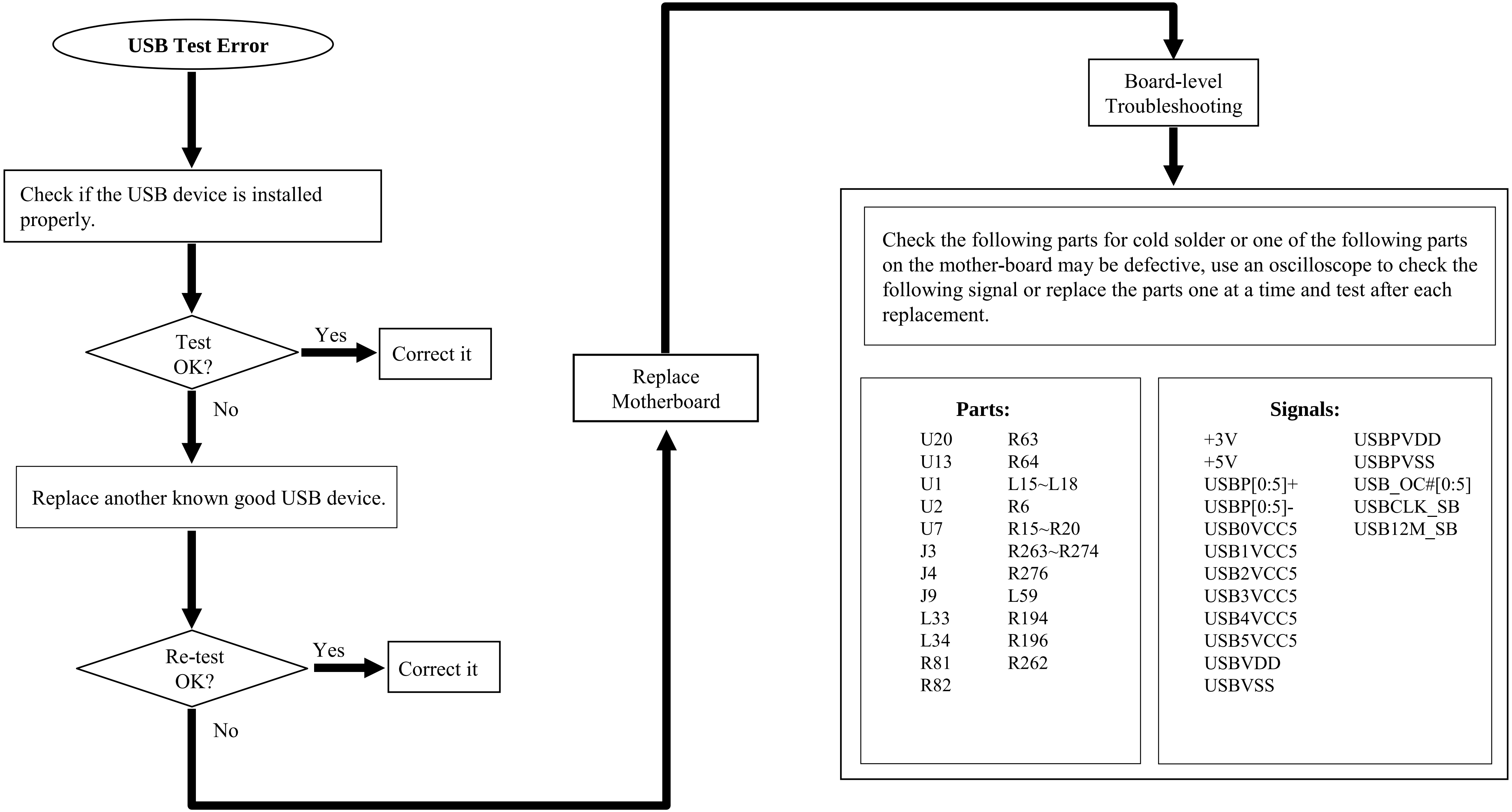
8.10 CD-ROM Drive Test Error (2)

An error message is shown when reading data from CD-ROM drive.


+5VS
J21
JS5
38,40,42
C313
0.1U
C314
0.1U
P15
+5VS
+5VS
+3VS
R331
10K
R327
10K
R338
150
D508
CL-190G
R347
0
CDROM_LED#
37
Q33
DTC144TKA
P12
IDERST#
5
PCIRST#
Q32
DTC144TKA
IDE_SDD[0:6,8:15]
6,8~22
IDE_SDD7
7
R328
5.6K
U20
SiS963L
SB
IDE_SDDREQ
22
IDE_SIORDY
27
IDE_IRQ15
29
IDE_SDIOW#
25
IDE_SDIOR#
24
IDE_SDDACK#
30
IDE_SDA[0:2]
31,33,34
IDE_SDCS3#
36
IDE_SDCS1#
35
Secondary EIDE Connector
4
23
26
43
44
45
46
48
GND1
GND2

8.11 USB Port Test Error (1)

An error occurs when a USB I/O device is installed.


USB Test Error
Check if the USB device is installed properly.
Test OK?
Yes
Correct it
No
Replace another known good USB device.
Re-test OK?
Yes
Correct it
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

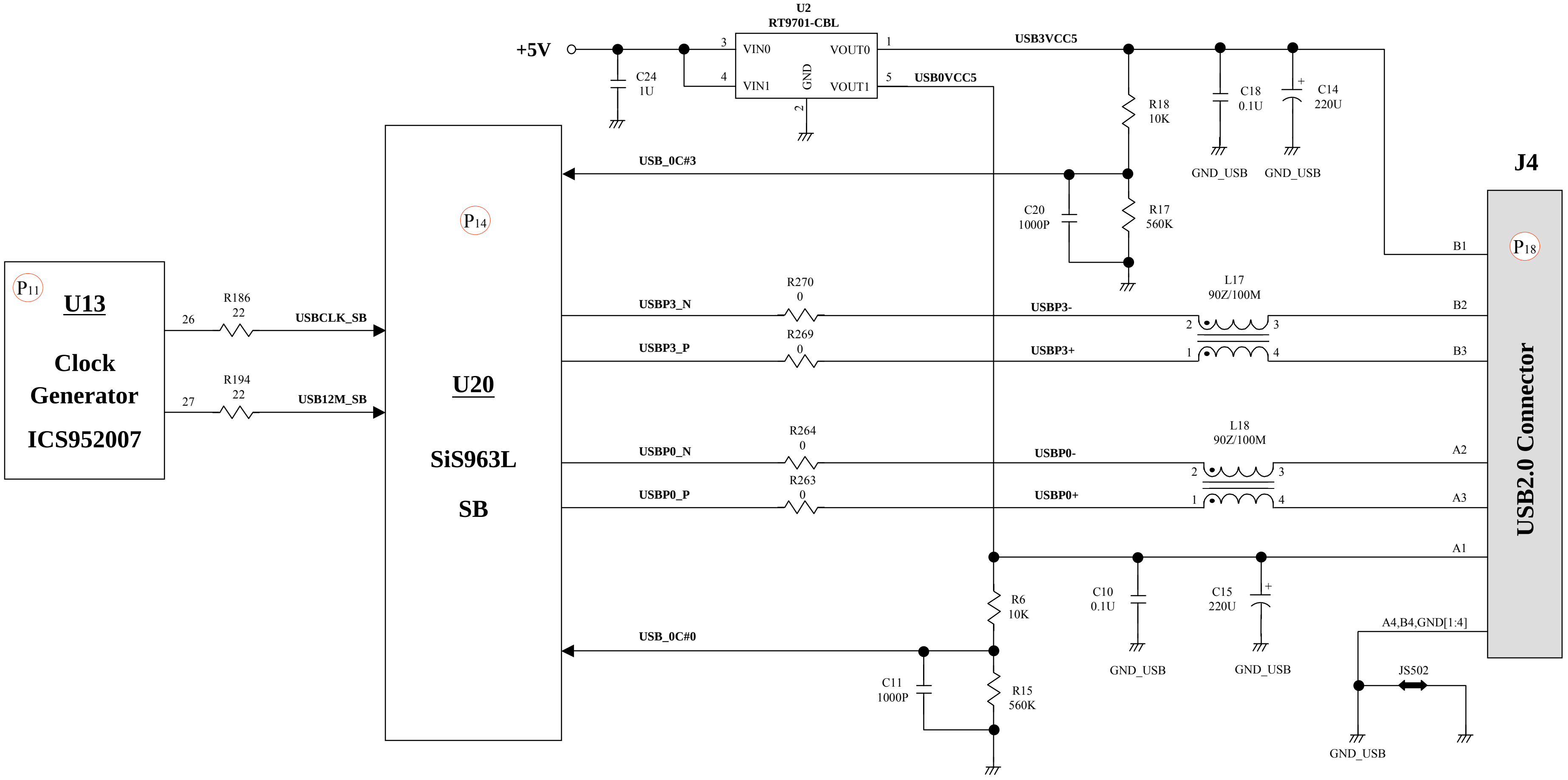
U20
U13
U1
U2
U7
J3
J4
J9
L33
L34
R81
R82
R63
R64
L15~L18
R6
R15~R20
R263~R274
R276
L59
R194
R196
R262

Signals:

+3V
+5V
USBP[0:5]+
USBP[0:5]-
USB0VCC5
USB1VCC5
USB2VCC5
USB3VCC5
USB4VCC5
USB5VCC5
USBVDD
USBVSS
USBPVDD
USBPVSS
USB_OC#[0:5]
USBCLK_SB
USB12M_SB

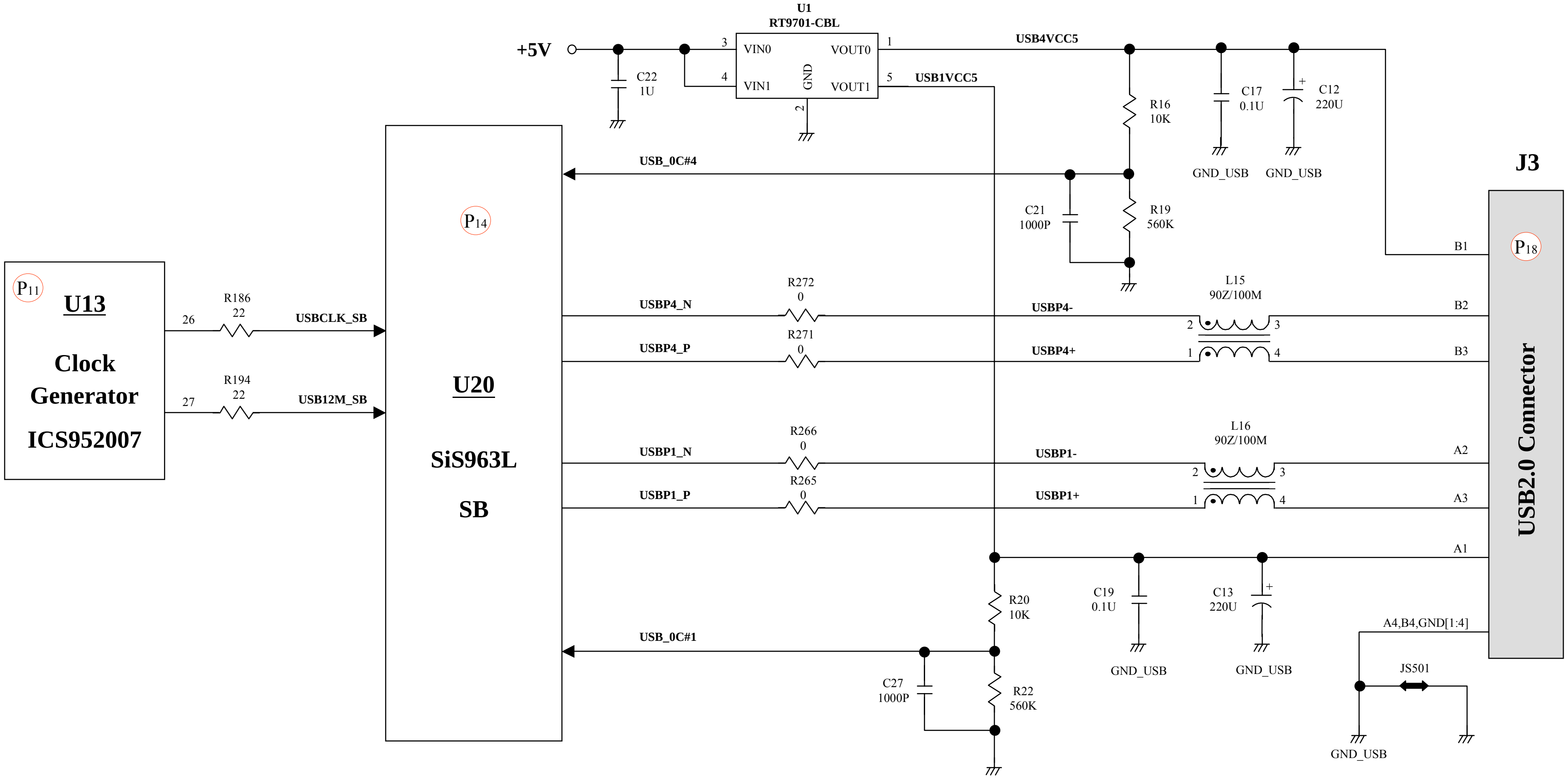
8.11 USB Port Test Error (2)

An error occurs when a USB I/O device is installed.


U2
RT9701-CBL
+5V
C24
1U
3
4
VIN0
VIN1
GND
2
VOUT0
VOUT1
1
5
USB3VCC5
USB0VCC5
R18
10K
C18
0.1U
C14
220U
GND_USB
GND_USB
J4
USB_0C#3
C20
1000P
R17
560K
P14
P11
U13
Clock
Generator
ICS952007
26
27
R186
22
USBCLK_SB
R194
22
USB12M_SB
U20
SiS963L
SB
P18
B1
L17
90Z/100M
R270
0
USBP3_N
USBP3-
B2
R269
0
USBP3_P
USBP3+
B3
L18
90Z/100M
R264
0
USBP0_N
USBP0-
A2
R263
0
USBP0_P
USBP0+
A3
A1
USB2.0 Connector
R6
10K
C10
0.1U
C15
220U
A4,B4,GND[1:4]
USB_0C#0
C11
1000P
R15
560K
GND_USB
GND_USB
JS502
GND_USB

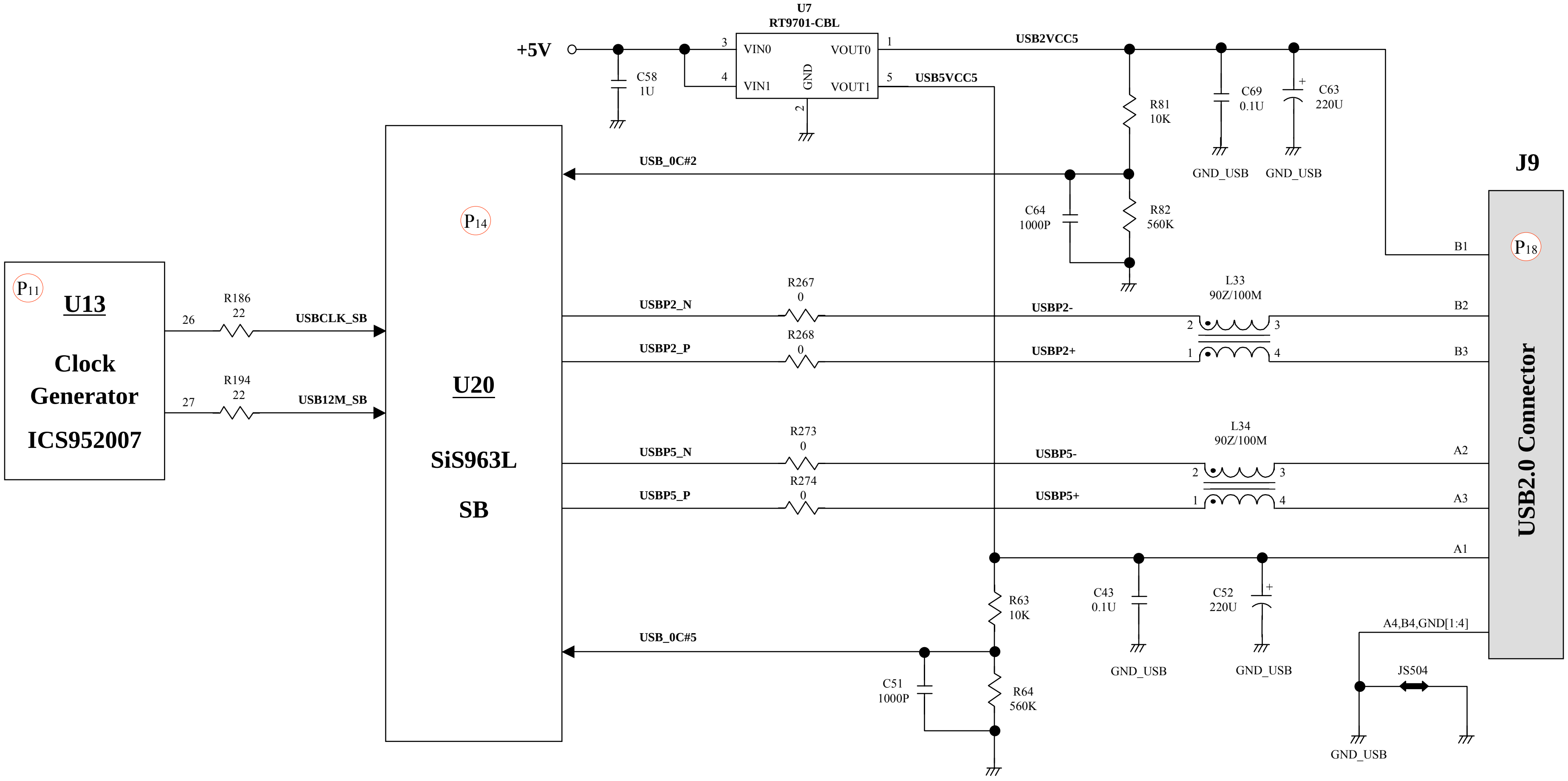
8.11 USB Port Test Error (3)

An error occurs when a USB I/O device is installed.


U1
RT9701-CBL
+5V
VIN0
VIN1
VOUT0
VOUT1
GND
3
4
2
1
5
C22
1U
USB4VCC5
USB1VCC5
R16
10K
C17
0.1U
C12
220U
GND_USB
GND_USB
J3
USB_0C#4
C21
1000P
R19
560K
P14
P11
U13
Clock
Generator
ICS952007
26
27
R186
22
USBCLK_SB
R194
22
USB12M_SB
U20
SiS963L
SB
USBP4_N
R272
0
USBP4_P
R271
0
USBP4-
USBP4+
L15
90Z/100M
USBP1_N
R266
0
USBP1_P
R265
0
USBP1-
USBP1+
L16
90Z/100M
B1
B2
B3
A2
A3
A1
A4,B4,GND[1:4]
P18
USB2.0 Connector
R20
10K
C19
0.1U
C13
220U
GND_USB
GND_USB
USB_0C#1
C27
1000P
R22
560K
JS501
GND_USB

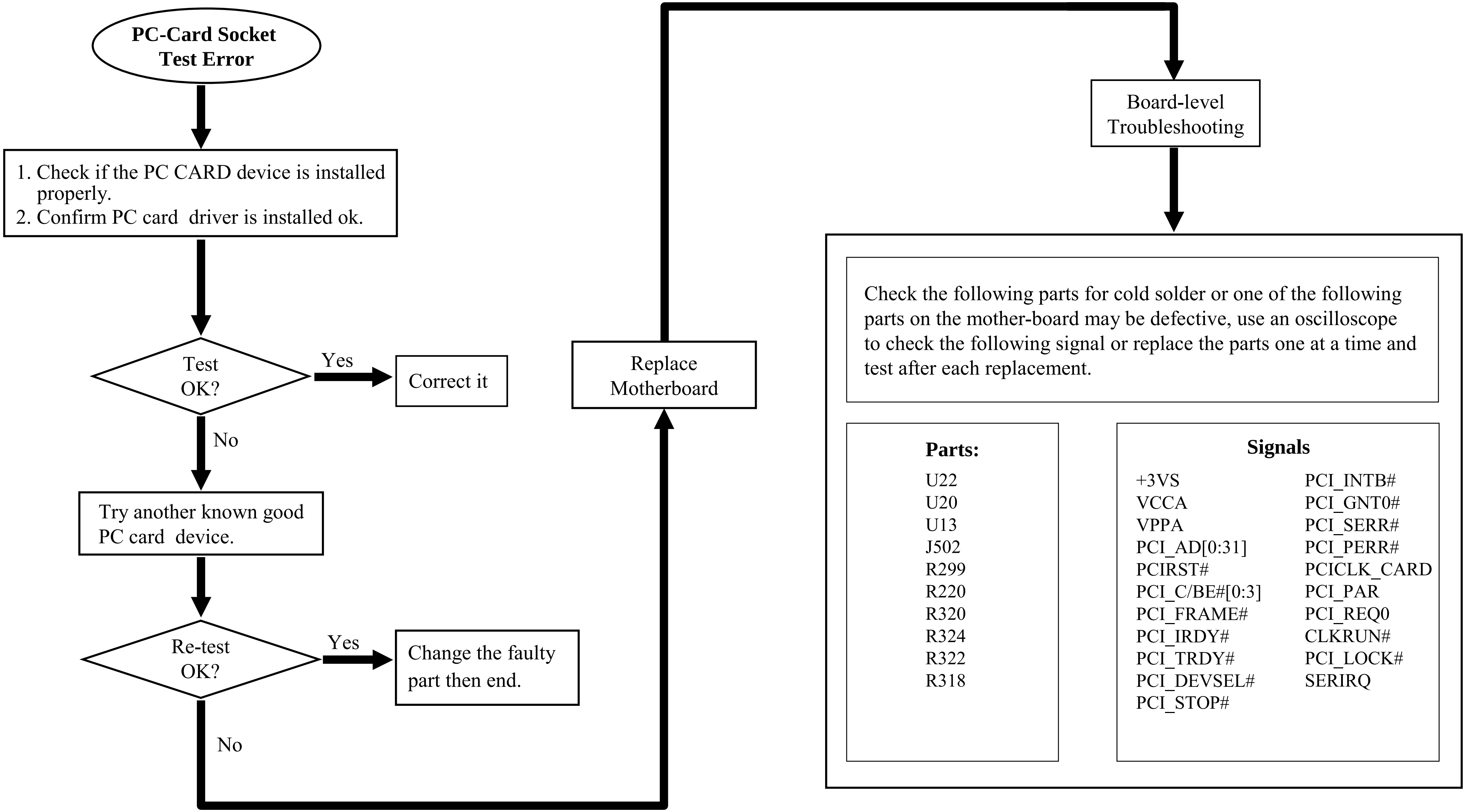
8.11 USB Port Test Error (4)

An error occurs when a USB I/O device is installed.


U7
RT9701-CBL
+5V
VIN0
VIN1
GND
VOUT0
VOUT1
3
4
2
1
5
C58
1U
USB2VCC5
USB5VCC5
R81
10K
C69
0.1U
C63
220U
GND_USB
GND_USB
J9
USB_0C#2
C64
1000P
R82
560K
P14
B1
P18
P11
U13
Clock
Generator
ICS952007
26
27
R186
22
R194
22
USBCLK_SB
USB12M_SB
U20
SiS963L
SB
USBP2_N
USBP2_P
R267
0
R268
0
USBP2-
USBP2+
L33
90Z/100M
B2
B3
USBP5_N
USBP5_P
R273
0
R274
0
USBP5-
USBP5+
L34
90Z/100M
A2
A3
A1
USB2.0 Connector
R63
10K
C43
0.1U
C52
220U
A4,B4,GND[1:4]
USB_0C#5
C51
1000P
R64
560K
GND_USB
GND_USB
JS504
GND_USB

8.12 PC Card Socket Test Error (1)

An error occurs when a PC card device is installed.


PC-Card Socket Test Error
Test OK?
Yes
Correct it
No
Try another known good PC card device.
Re-test OK?
Yes
Change the faulty part then end.
No
Replace Motherboard
Board-level Troubleshooting

1. Check if the PC CARD device is installed properly.
2. Confirm PC card driver is installed ok.

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

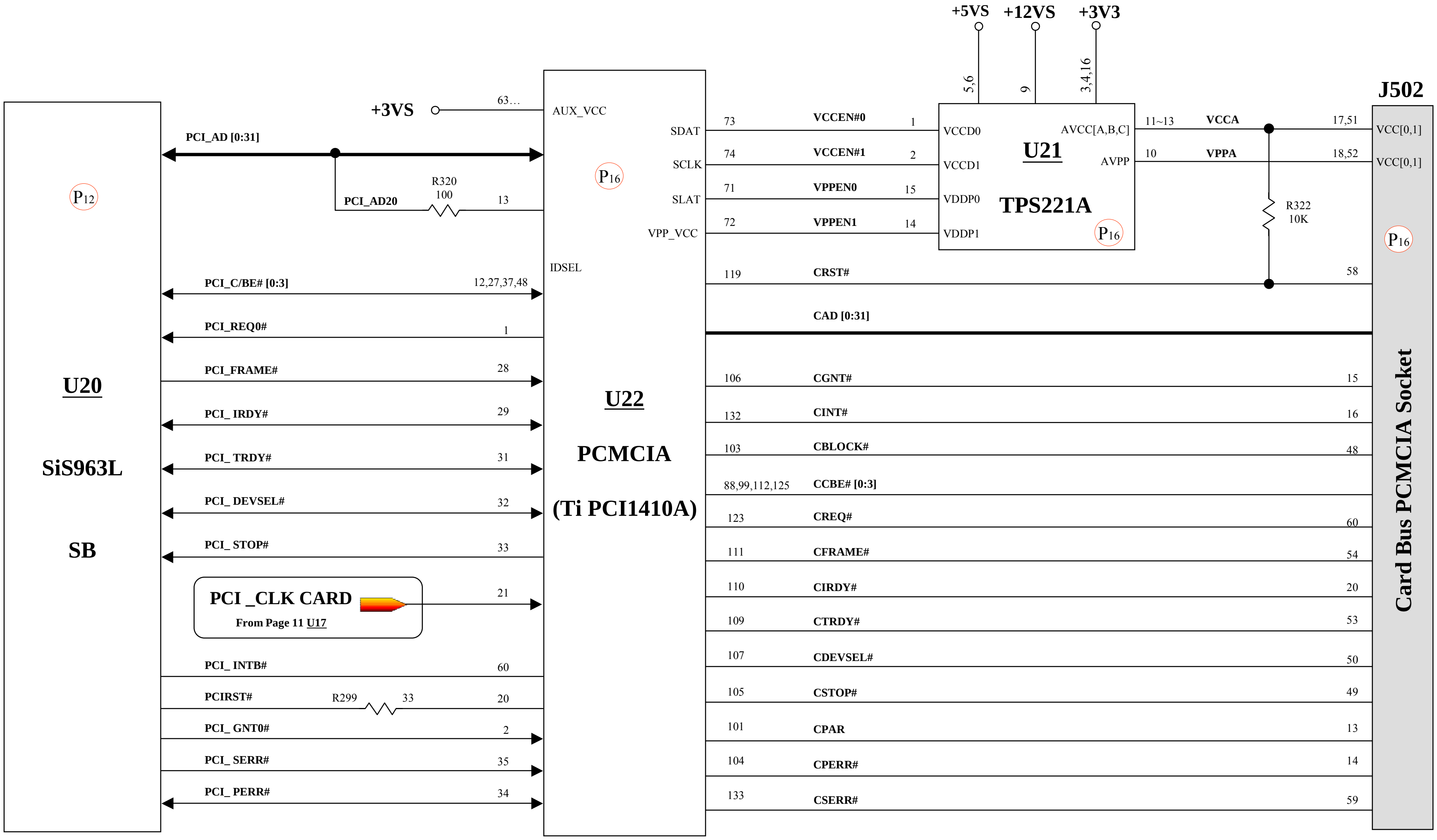
U22
U20
U13
J502
R299
R220
R320
R324
R322
R318

Signals

+3VS
VCCA
VPPA
PCI_AD[0:31]
PCIRST#
PCI_C/BE#[0:3]
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_DEVSEL#
PCI_STOP#
PCI_INTB#
PCI_GNT0#
PCI_SERR#
PCI_PERR#
PCICLK_CARD
PCI_PAR
PCI_REQ0
CLKRUN#
PCI_LOCK#
SERIRQ

8.12 PC Card Socket Test Error (2)

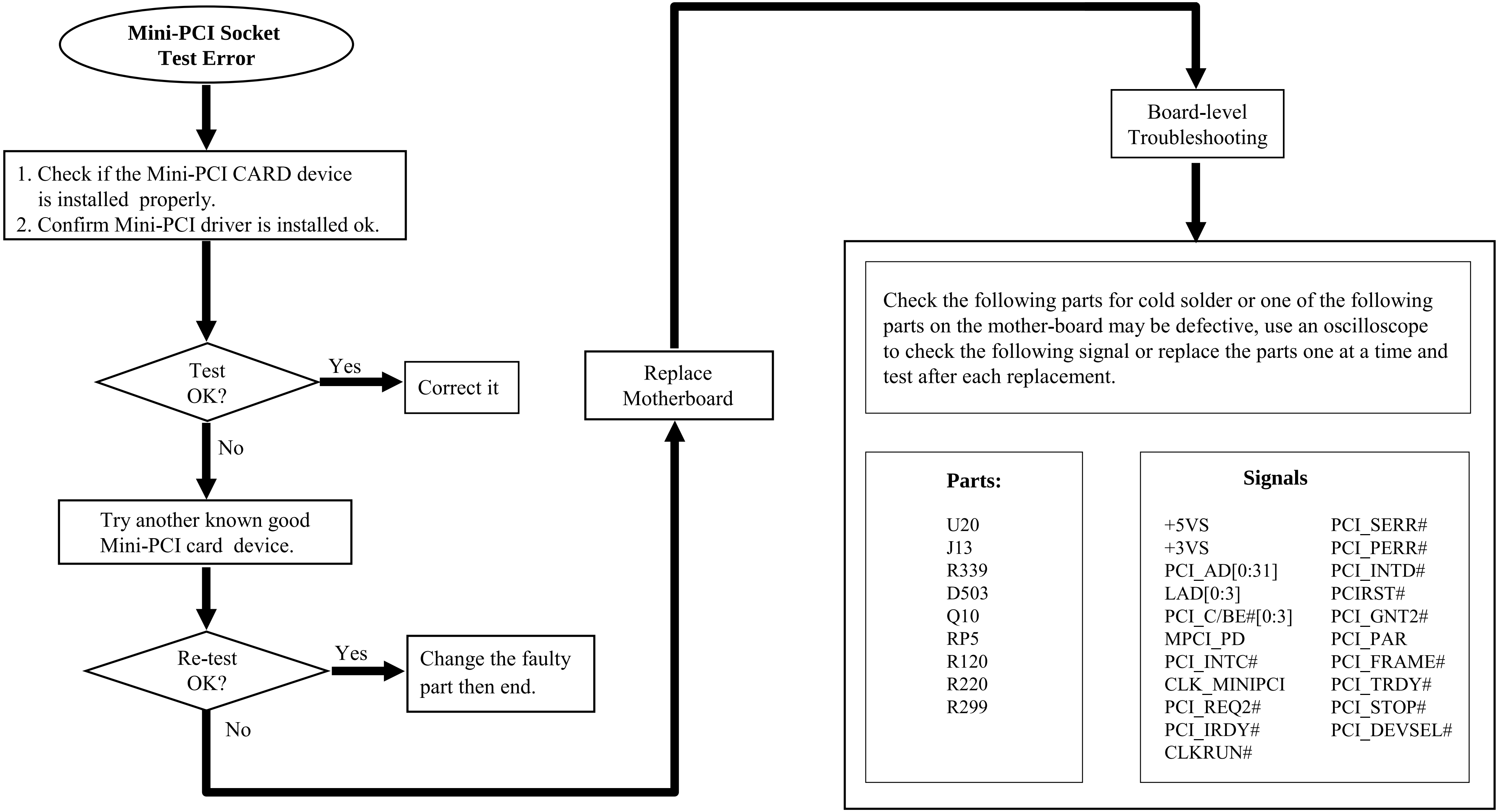
An error occurs when a PC card device is installed.



+5VS
+12VS
+3V3
5,6
9
3,4,16
J502
+3VS
63…
AUX_VCC
PCI_AD [0:31]
SDAT
SCLK
SLAT
VPP_VCC
P16
P12
R320
100
PCI_AD20
13
IDSEL
73
VCCEN#0
1
74
VCCEN#1
2
71
VPPEN0
15
72
VPPEN1
14
VCCD0
VCCD1
VDDP0
VDDP1
U21
TPS221A
AVCC[A,B,C]
AVPP
11~13
VCCA
10
VPPA
17,51
18,52
VCC[0,1]
VCC[0,1]
R322
10K
119
CRST#
58
CAD [0:31]
PCI_C/BE# [0:3]
12,27,37,48
PCI_REQ0#
1
PCI_FRAME#
28
PCI_ IRDY#
29
PCI_ TRDY#
31
PCI_ DEVSEL#
32
PCI_ STOP#
33
PCI _CLK CARD
From Page 11 U17
21
PCI_ INTB#
60
PCIRST#
R299
33
20
PCI_ GNT0#
2
PCI_ SERR#
35
PCI_ PERR#
34
U20
SiS963L
SB
U22
PCMCIA
(Ti PCI1410A)
106
CGNT#
15
132
CINT#
16
103
CBLOCK#
48
88,99,112,125
CCBE# [0:3]
123
CREQ#
60
111
CFRAME#
54
110
CIRDY#
20
109
CTRDY#
53
107
CDEVSEL#
50
105
CSTOP#
49
101
CPAR
13
104
CPERR#
14
133
CSERR#
59
Card Bus PCMCIA Socket

8.13 Mini-PCI Socket Test Error (1)

An error occurs when a PC card device is installed.


Mini-PCI Socket Test Error
1. Check if the Mini-PCI CARD device is installed properly.
2. Confirm Mini-PCI driver is installed ok.
Test OK?
Yes
Correct it
No
Try another known good Mini-PCI card device.
Re-test OK?
Yes
Change the faulty part then end.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

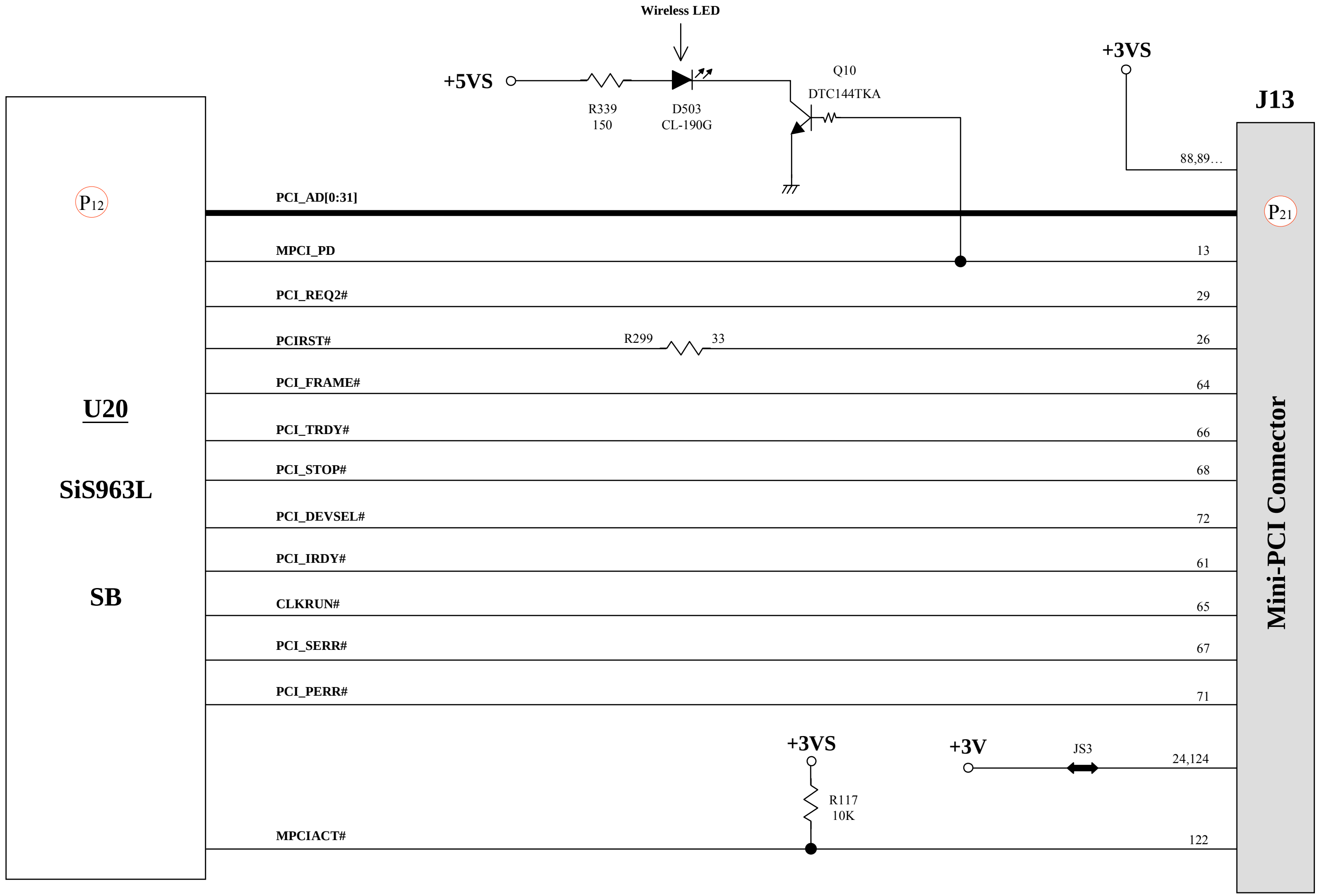
U20
J13
R339
D503
Q10
RP5
R120
R220
R299

Signals

+5VS
+3VS
PCI_AD[0:31]
LAD[0:3]
PCI_C/BE#[0:3]
MPCI_PD
PCI_INTC#
CLK_MINIPCI
PCI_REQ2#
PCI_IRDY#
CLKRUN#
PCI_SERR#
PCI_PERR#
PCI_INTD#
PCIRST#
PCI_GNT2#
PCI_PAR
PCI_FRAME#
PCI_TRDY#
PCI_STOP#
PCI_DEVSEL#

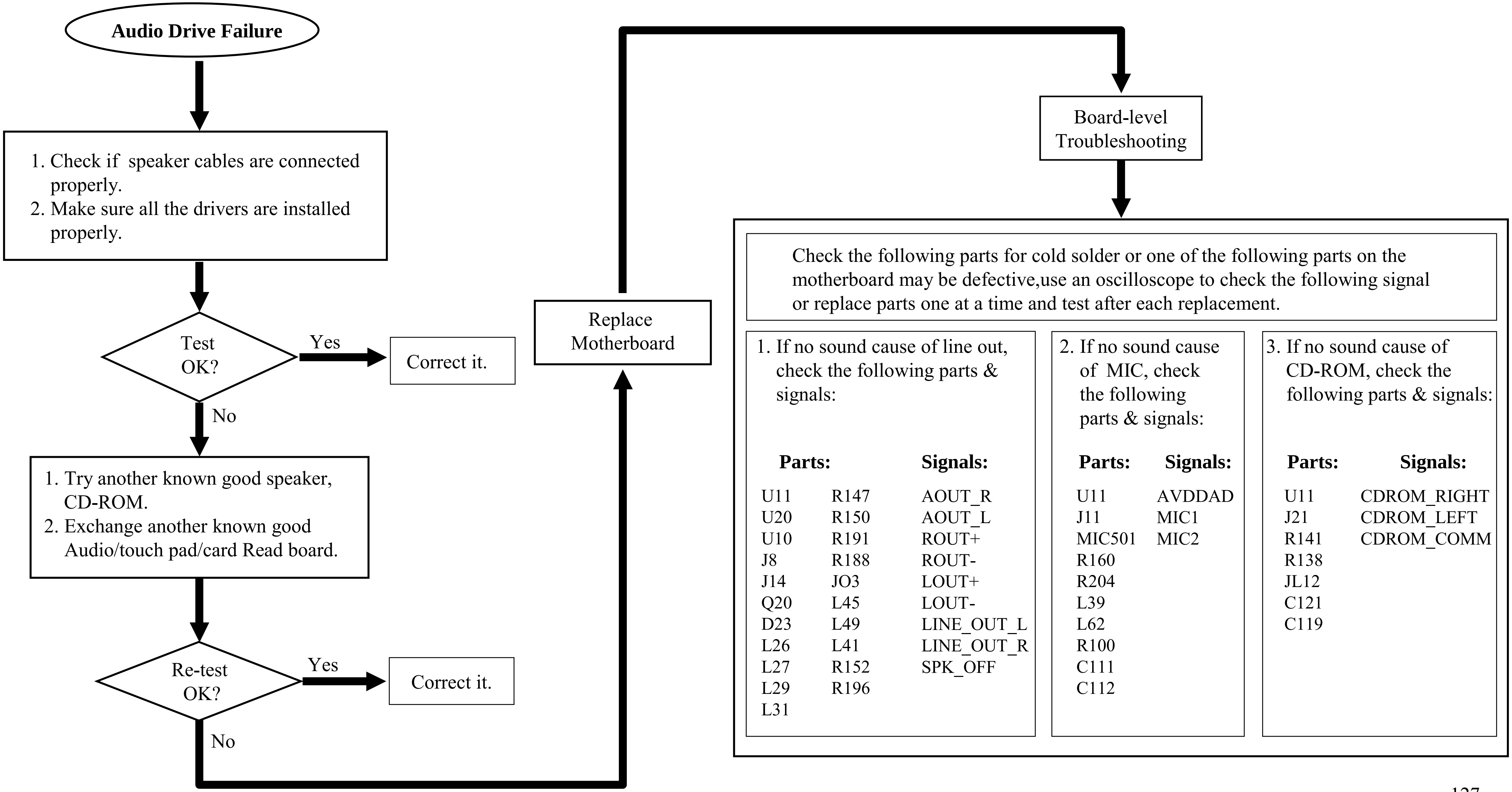
8.13 Mini-PCI Socket Test Error (2)

An error occurs when a PC card device is installed.


Wireless LED
+5VS
R339
150
D503
CL-190G
Q10
DTC144TKA
+3VS
J13
88,89…
P12
PCI_AD[0:31]
P21
MPCI_PD
13
PCI_REQ2#
29
PCIRST#
R299
33
26
PCI_FRAME#
64
U20
PCI_TRDY#
66
PCI_STOP#
68
SiS963L
PCI_DEVSEL#
72
PCI_IRDY#
61
SB
CLKRUN#
65
PCI_SERR#
67
PCI_PERR#
71
Mini-PCI Connector
+3VS
+3V
JS3
24,124
R117
10K
MPCIACT#
122

8.14 Audio Failure (1)

No sound from speaker after audio driver is installed.



Audio Drive Failure

1. Check if speaker cables are connected properly.
2. Make sure all the drivers are installed properly.

Test OK? Yes → Correct it.

No →

1. Try another known good speaker, CD-ROM.
2. Exchange another known good Audio/touch pad/card Read board.

Re-test OK? Yes → Correct it.

No → Replace Motherboard → Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the motherboard may be defective,use an oscilloscope to check the following signal or replace parts one at a time and test after each replacement.

1. If no sound cause of line out, check the following parts & signals:

Parts:		**Signals:**
U11	R147	AOUT_R
U20	R150	AOUT_L
U10	R191	ROUT+
J8	R188	ROUT-
J14	JO3	LOUT+
Q20	L45	LOUT-
D23	L49	LINE_OUT_L
L26	L41	LINE_OUT_R
L27	R152	SPK_OFF
L29	R196	
L31		

2. If no sound cause of MIC, check the following parts & signals:

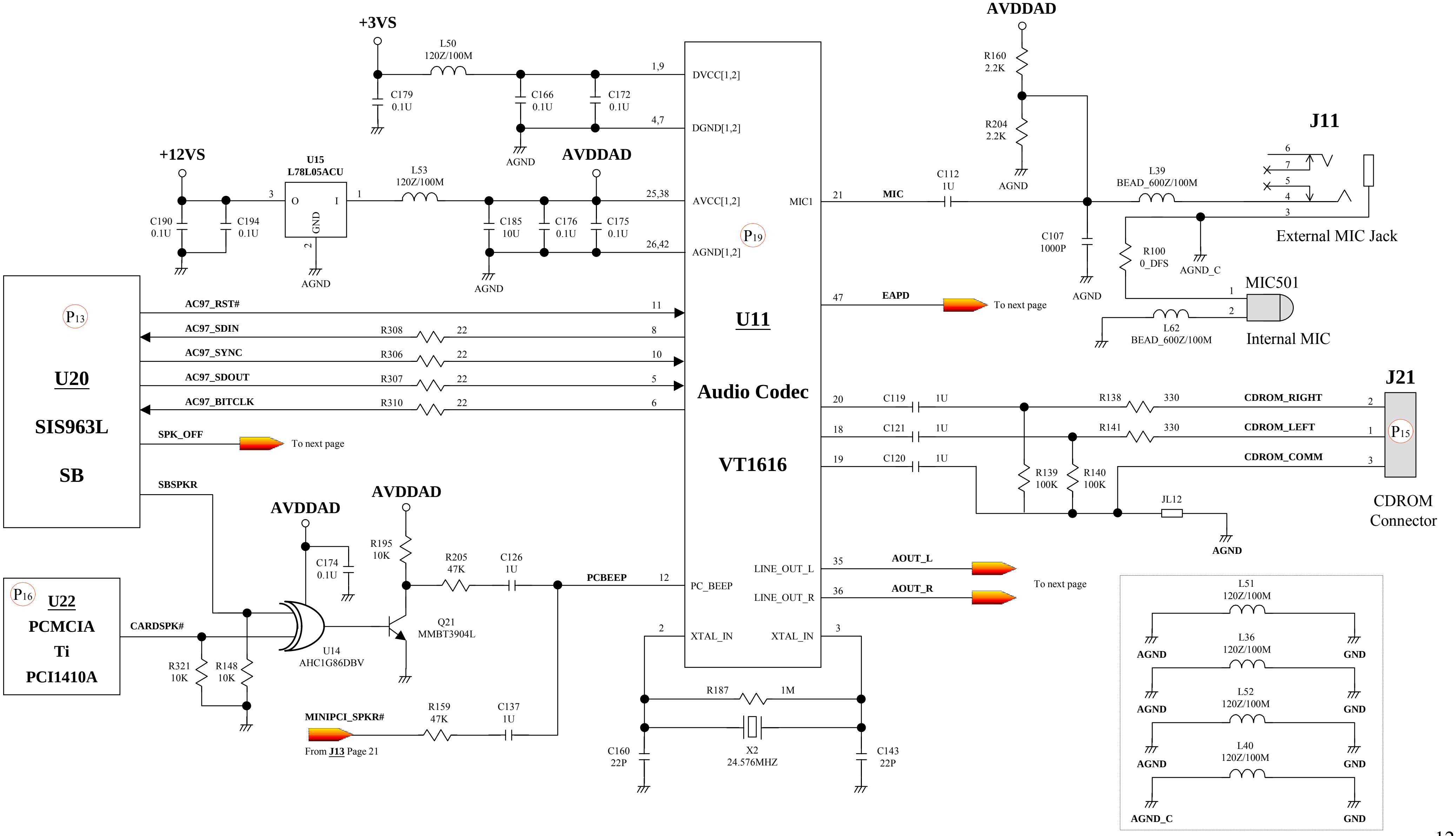
Parts:	**Signals:**
U11	AVDDAD
J11	MIC1
MIC501	MIC2
R160	
R204	
L39	
L62	
R100	
C111	
C112	

3. If no sound cause of CD-ROM, check the following parts & signals:

Parts:	**Signals:**
U11	CDROM_RIGHT
J21	CDROM_LEFT
R141	CDROM_COMM
R138	
JL12	
C121	
C119	

8.14 Audio Failure (2) – Audio IN

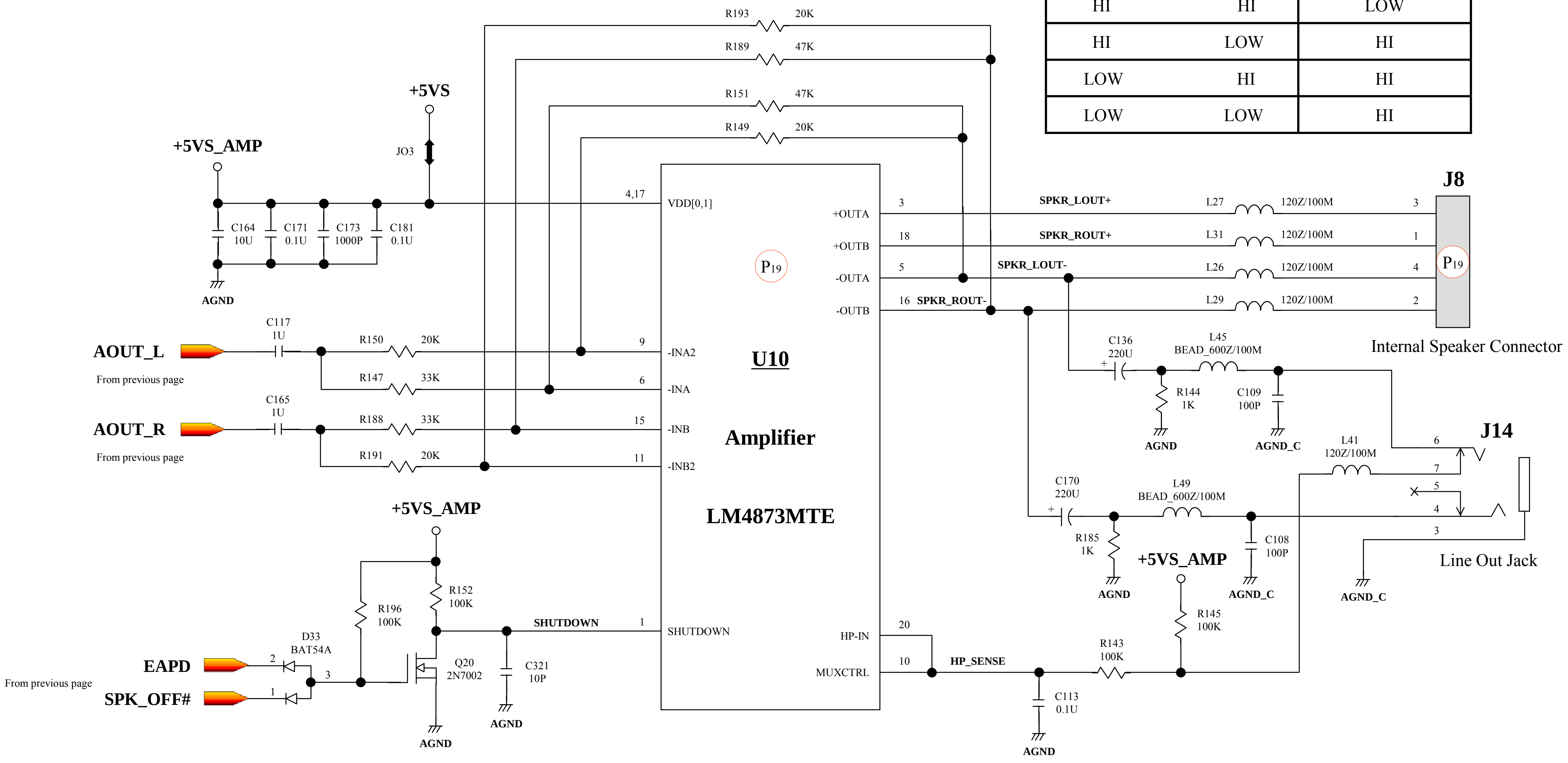
No sound from speaker after audio driver is installed.


+3VS
L50
120Z/100M
C179
0.1U
C166
0.1U
C172
0.1U
1,9
4,7
AGND
+12VS
U15
L78L05ACU
3
O
I
1
GND
2
C190
0.1U
C194
0.1U
AGND
L53
120Z/100M
AVDDAD
C185
10U
C176
0.1U
C175
0.1U
25,38
26,42
AGND
DVCC[1,2]
DGND[1,2]
AVCC[1,2]
AGND[1,2]
MIC1
P19
U11
Audio Codec
VT1616
P13
U20
SIS963L
SB
AC97_RST#
11
AC97_SDIN
R308
22
8
AC97_SYNC
R306
22
10
AC97_SDOUT
R307
22
5
AC97_BITCLK
R310
22
6
SPK_OFF
To next page
SBSPKR
AVDDAD
AVDDAD
C174
0.1U
R195
10K
R205
47K
C126
1U
PCBEEP
12
PC_BEEP
Q21
MMBT3904L
U14
AHC1G86DBV
P16
U22
PCMCIA
Ti
PCI1410A
CARDSPK#
R321
10K
R148
10K
MINIPCI_SPKR#
From J13 Page 21
R159
47K
C137
1U
2
XTAL_IN
XTAL_IN
3
R187
1M
X2
24.576MHZ
C160
22P
C143
22P
LINE_OUT_L
LINE_OUT_R
35
AOUT_L
36
AOUT_R
To next page
AVDDAD
R160
2.2K
R204
2.2K
AGND
21
MIC
C112
1U
C107
1000P
AGND
L39
BEAD_600Z/100M
J11
6
7
5
4
3
External MIC Jack
R100
0_DFS
AGND_C
MIC501
1
2
L62
BEAD_600Z/100M
Internal MIC
47
EAPD
To next page
J21
20
C119
1U
R138
330
CDROM_RIGHT
2
18
C121
1U
R141
330
CDROM_LEFT
1
19
C120
1U
CDROM_COMM
3
P15
R139
100K
R140
100K
JL12
AGND
CDROM
Connector
L51
120Z/100M
AGND
GND
L36
120Z/100M
AGND
GND
L52
120Z/100M
AGND
GND
L40
120Z/100M
AGND_C
GND

8.14 Audio Failure (3) – Audio OUT

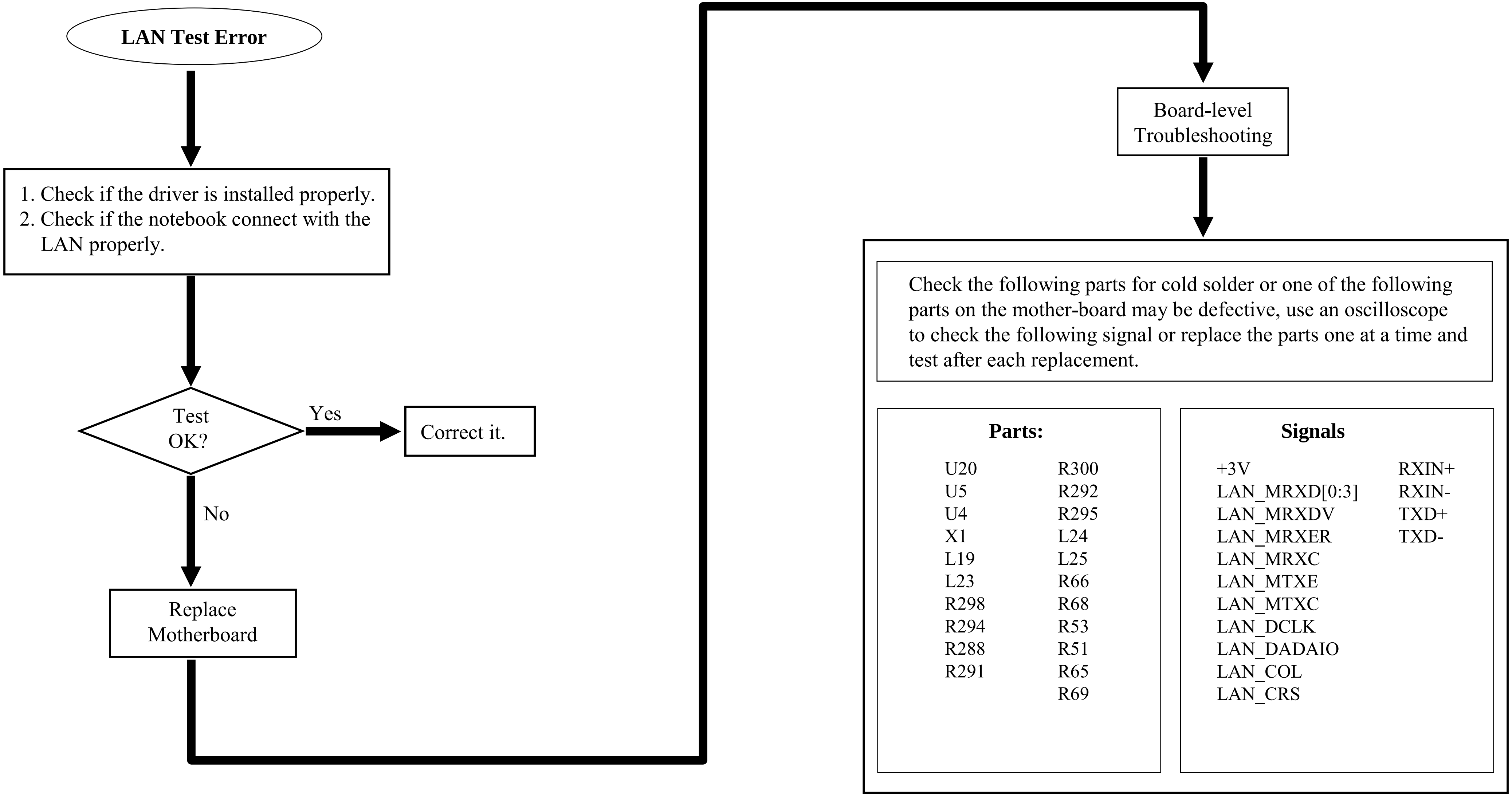
No sound from speaker after audio driver is installed.

SPK_OFF#	EAPD	SHUTDOWN
HI	HI	LOW
HI	LOW	HI
LOW	HI	HI
LOW	LOW	HI


R193 20K
R189 47K
R151 47K
R149 20K
+5VS
JO3
+5VS_AMP
4,17
VDD[0,1]
C164 10U
C171 0.1U
C173 1000P
C181 0.1U
AGND
C117 1U
AOUT_L
From previous page
R150 20K
R147 33K
C165 1U
AOUT_R
From previous page
R188 33K
R191 20K
9 -INA2
6 -INA
15 -INB
11 -INB2
U10
Amplifier
LM4873MTE
P19
+OUTA 3
+OUTB 18
-OUTA 5
-OUTB 16
SPKR_LOUT+
SPKR_ROUT+
SPKR_LOUT-
SPKR_ROUT-
L27 120Z/100M
L31 120Z/100M
L26 120Z/100M
L29 120Z/100M
J8
3
1
4
2
P19
Internal Speaker Connector
C136 220U
L45 BEAD_600Z/100M
R144 1K
C109 100P
AGND
AGND_C
L41 120Z/100M
J14
6
7
5
4
3
Line Out Jack
AGND_C
C170 220U
L49 BEAD_600Z/100M
R185 1K
C108 100P
AGND
AGND_C
+5VS_AMP
R145 100K
R143 100K
HP_SENSE
C113 0.1U
AGND
20 HP-IN
10 MUXCTRL
1 SHUTDOWN
SHUTDOWN
+5VS_AMP
R152 100K
R196 100K
D33 BAT54A
Q20 2N7002
C321 10P
AGND
AGND
EAPD
SPK_OFF#
From previous page
2
1
3

8.15 LAN Test Error (1)

An error occurs when a LAN device is installed.


LAN Test Error
1. Check if the driver is installed properly.
2. Check if the notebook connect with the LAN properly.
Test OK?
Yes
Correct it.
No
Replace Motherboard
Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

Parts:

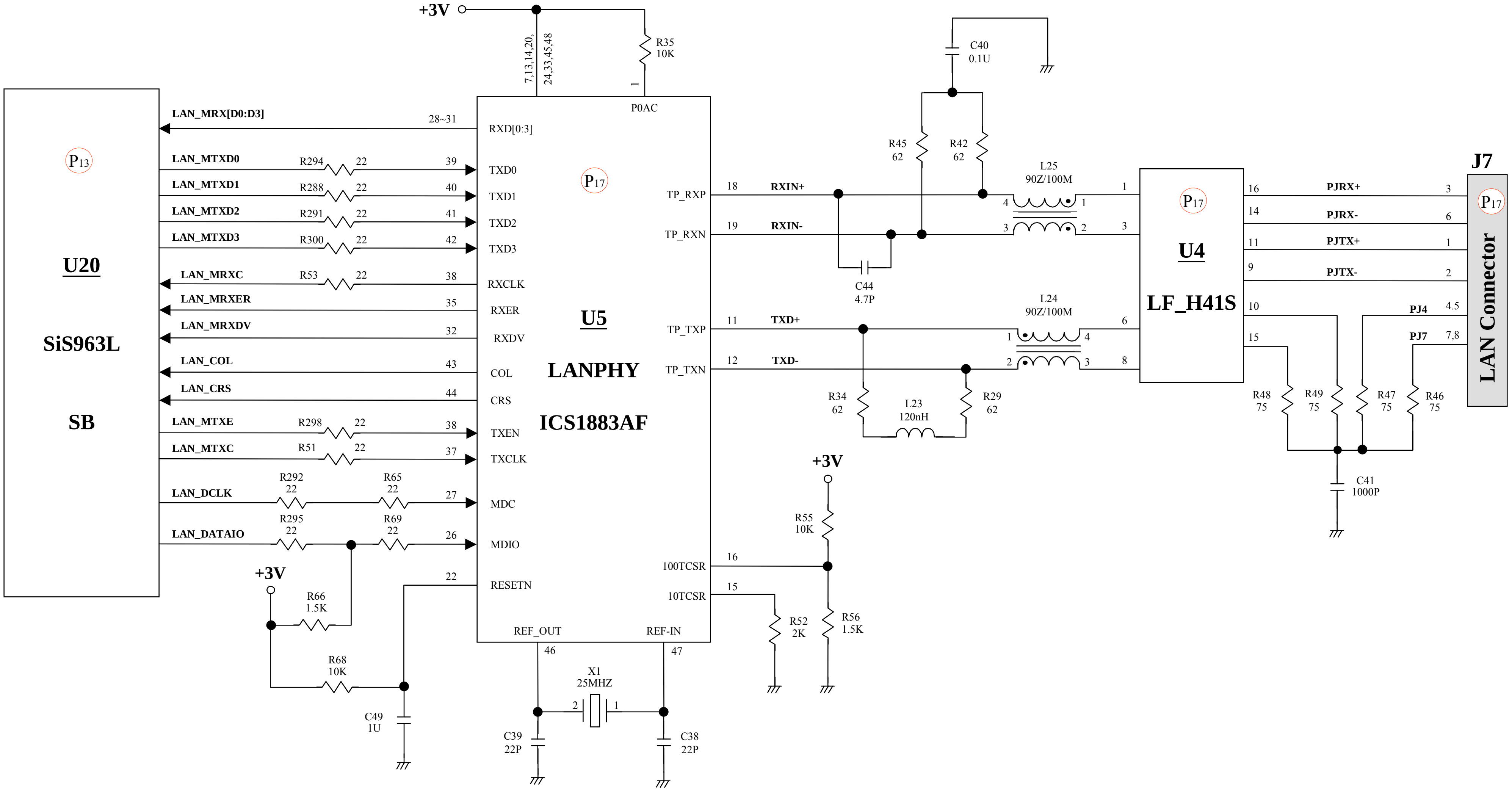
U20
U5
U4
X1
L19
L23
R298
R294
R288
R291
R300
R292
R295
L24
L25
R66
R68
R53
R51
R65
R69

Signals

+3V
LAN_MRXD[0:3]
LAN_MRXDV
LAN_MRXER
LAN_MRXC
LAN_MTXE
LAN_MTXC
LAN_DCLK
LAN_DADAIO
LAN_COL
LAN_CRS
RXIN+
RXIN-
TXD+
TXD-

8.15 LAN Test Error (2)

An error occurs when a LAN device is installed.


+3V
7,13,14,20,
24,33,45,48
R35
10K
1
P0AC
C40
0.1U
U20
SiS963L
SB
P13
LAN_MRX[D0:D3]
LAN_MTXD0
LAN_MTXD1
LAN_MTXD2
LAN_MTXD3
LAN_MRXC
LAN_MRXER
LAN_MRXDV
LAN_COL
LAN_CRS
LAN_MTXE
LAN_MTXC
LAN_DCLK
LAN_DATAIO
R294 22
R288 22
R291 22
R300 22
R53 22
R298 22
R51 22
R292 22
R65 22
R295 22
R69 22
28~31
39
40
41
42
38
35
32
43
44
38
37
27
26
22
RXD[0:3]
TXD0
TXD1
TXD2
TXD3
RXCLK
RXER
RXDV
COL
CRS
TXEN
TXCLK
MDC
MDIO
RESETN
REF_OUT
REF-IN
P17
U5
LANPHY
ICS1883AF
TP_RXP
TP_RXN
TP_TXP
TP_TXN
100TCSR
10TCSR
18
19
11
12
16
15
46
47
RXIN+
RXIN-
TXD+
TXD-
R45
62
R42
62
C44
4.7P
L25
90Z/100M
L24
90Z/100M
R34
62
R29
62
L23
120nH
+3V
R55
10K
R52
2K
R56
1.5K
+3V
R66
1.5K
R68
10K
C49
1U
X1
25MHZ
C39
22P
C38
22P
U4
LF_H41S
P17
16
14
11
9
10
15
PJRX+
PJRX-
PJTX+
PJTX-
PJ4
PJ7
3
6
1
2
4.5
7,8
R48
75
R49
75
R47
75
R46
75
C41
1000P
J7
P17
LAN Connector

9. Spare Parts List

Spare Part List 1

Part Number	Description	Location(S)
221679920001	CARTON;NON-BRAND,8640C	
221679950001	PARTITION;IN CARTON,8640C	
221679950002	CARD BOARD;TOP/BTM,PALLET,8640C	
221679950003	CARD BOARD;FRAME,PALLET,8640C	
221679950004	PARTITION;PALLET,8640C	
222600020049	PE BAG;50*70MM,W/SEAL,COMMON	
222600020310	PE BAG;70X100MM,W/SEAL,COMMON	
222670820003	PE BAG;L560*W345,7521N	
222671330003	PE BAG;LCD BRACKET,STINGRAY	
222678500002	PE BUBBLE BAG;BATTERY,280*170,MS	
224670830002	PALLET;1250*1080*130,7521N	
225600000054	TAPE;INSULATING,POLYESTER FILM,1	
225600000061	TAPE;ADHENSIVE,DOUBLE-FACE,W20,U	
225682900001	CONDUCTIVE TAPE;DC,M/B,8599	
227675400003	EPE PAD;K/B,8355	
227682900001	END CAP;R,8599	
227682900002	END CAP;L,8599	
242600000001	LABEL;PAL,20*5MM,COMMON	
242600000088	LABEL;BAR CODE,125*65,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000145	LABEL;10*10,BLANK,COMMON	
242600000232	LABEL;6*6MM,GAL,BLANK,COMMON	
242600000378	LABEL;27*7MM,HI-TEMP 260'C	
242600000433	LABEL;BLANK,11*5MM,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000439	LABEL;25*6,HI-TEMP,COMMON	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242600000452	LABEL;BLANK,7MM*7MM,PRC	
242664800013	LABEL;CAUTION,INVERT BD,PITCHING	
242668300028	LABEL;32*7MM,POLYESTER FILM,HOPE	
242669600005	LABEL;LOT NUMBER,RACE	
242670800113	BFM-WORLD MARK;WINXP,7521N	
242679900005	LABEL;BAR CODE,(25*10MM)*12pcs,8	
242682900001	LABEL;AGENCY-GLOBAL,8599	
242682900005	LABEL;BATT 14.8V/4AH,LI,PANA,MSL	
271002103301	RES;10K ,1/10W,5% ,0805,SMT	PR114,PR54,PR55
271002104301	RES;100K ,1/10W,5% ,0805,SMT	PR110
271002331301	RES;330 ,1/10W,5% ,0805,SMT	FR3,FR4,R14,R15
271013102301	RES;1K ,1/4W ,5% ,1206,SMT	PR166,PR167
271013221301	RES;220 ,1/4W,5% ,1206,SMT	PR118,PR157,PR158,PR159
271044060301	RES;.006 ,1.5W,5% ,2512,SMT	
271044061101	RES;.06,2W,1%,2512,SMT,乾坤	
271045057101	RES;.005 ,1W,1% ,2512,SMT	PR72
271045107101	RES;.01 ,1W ,1% ,2512,SMT	PR108,PR71
271045157101	RES;.015 ,1W ,1% ,2512,SMT	PR95
271045357101	RES;.035,1W,1%,2512,SMT	PR136
271046068101	RES;.006 ,1.5W ,1% ,2512,SMT;PWR	RM4
271046069101	RES;.06,2W,1%,2512,SMT	PR47,PR48
271061000002	RES;0 ,1/16W,0402,SMT	PC106,PC86,PR12,PR143,PR145,
271061100501	RES;10 ,1/16W,5% ,0402,SMT	PR52,PR59,PR63,R182,R199,R22

8599 N/B Maintenance

9. Spare Parts List

Spare Part List 2

Part Number	Description	Location(S)
271061101103	RES;100 ,1/16W,1% ,0402,SMT	R120,R124,R130,R320,R325,R326
271061102105	RES;1K ,1/16W,1% ,0402,SMT	PR105,PR92,R1,R144,R185,R2,R2
271061103102	RES;10K ,1/16W,1% ,0402,SMT	PR10,PR137,PR141,PR8,R146,R1
271061103501	RES;10K ,1/16W,5% ,0402,SMT	PR20,PR25,PR7,R117,R133,R134,
271061104102	RES;100K ,1/16W,1% ,0402,SMT	PR115,PR130
271061104501	RES;100K ,1/16W,5% ,0402,SMT	PR107,PR112,PR129,PR3,PR32,P
271061105501	RES;1M ,1/16W,5% ,0402,SMT	PR106,PR111,PR113,PR70,PR85,
271061121312	RES;12.1K,1/16W,1% ,0402,SMT	PR124
271061130111	RES;130 ,1/16W,1% ,0402,SMT	R131
271061151102	RES;150 ,1/16W, 1%,0402,SMT	R110,R211,R224,R230,R232,R234
271061152302	RES;15K ,1/16W,5% ,0402,SMT	R317
271061152501	RES;1.5K ,1/16W,5% ,0402,SMT	R333,R56,R66
271061202102	RES;2K ,1/16W,1% ,0402,SMT	R52
271061203102	RES;20K ,1/16W,1% ,0402,SMT	PR102,PR34,PR76,PR81,PR96,R1
271061220501	RES;22 ,1/16W,5% ,0402,SMT	R127,R128,R179,R180,R186,R194
271061222501	RES;2.2K ,1/16W,5% ,0402,SMT	R136,R153,R160,R91,R92
271061243101	RES;24K ,1/16W,1% ,0402,SMT	R73
271061261211	RES;26.1K,1/16W,1%,0402,SMT	PR77
271061272102	RES;2.7K ,1/16W,1% ,0402,SMT	R204
271061273501	RES;27K ,1/16W,5% ,0402,SMT	PR37
271061330501	RES;33 ,1/16W,5% ,0402,SMT	R173,R174,R175,R176,R200,R201
271061333101	RES;33K ,1/16W,1% ,0402,SMT	R147,R188
271061402011	RES;40.2 ,1/16W,1% ,0402,SMT	R235,R236
271061471501	RES;470 ,1/16W,5% ,0402,SMT	PR1,R210
271061472501	RES;4.7K ,1/16W,5% ,0402,SMT	R142,R155,R177,R178,R192,R246
271061473102	RES;47K ,1/16W,1% ,0402,SMT	R151,R189
271061473501	RES;47K ,1/16W,5% ,0402,SMT	PR131,PR2,R159,R315,R318
271061474501	RES;470K ,1/16W,5% ,0402,SMT	PR121,PR14,PR19,PR56,PR62,PR
271061475111	RES;475 ,1/16W,1% ,0402,SMT	R168
271061475211	RES;4.75K,1/16W,1% ,0402,SMT	PR104,PR75
271061499012	RES;49.9 ,1/16W,1% ,0402,SMT	R162,R163,R164,R165,R166,R167
271061512102	RES;5.1K ,1/16W,1% ,0402,SMT	PR38
271061562501	RES;5.6K ,1/16W,5% ,0402,SMT	R297,R328
271061564101	RES;560K ,1/16W,1% ,0402,SMT	R15,R17,R19,R22,R64,R82
271061620101	RES;62 ,1/16W,1% ,0402,SMT	R103,R104,R105,R106,R107,R108
271061681501	RES;680 ,1/16W,5% ,0402,SMT	R102
271061753101	RES;75,1/16W,1%,0402,SMT	R122,R46,R47,R48,R49
271071000002	RES;0 ,1/16W,5% ,0603,SMT	PR13,PR138,PR140,PR156,PR6
271071010301	RES;1 ,1/16W,5% ,0603,SMT	PR148,PR150
271071100302	RES;10 ,1/16W,5% ,0603,SMT	PR117,PR120,PR139,PR146,R21
271071101301	RES;100 ,1/16W,5% ,0603,SMT	R11,R12,R13,R17,R18,R35,R36,R4
271071102102	RES;1K ,1/16W,1% ,0603,SMT	PR149,PR160,PR79,PR99
271071102302	RES;1K ,1/16W,5% ,0603,SMT	R11
271071103302	RES;10K ,1/16W,5% ,0603,SMT	R1,R37,R38
271071104101	RES;100K ,1/16W,1% ,0603,SMT	R2,R3
271071104101	RES;100K ,1/16W,1% ,0603,SMT	PR128,PR142,PR151,PR153
271071104302	RES;100K ,1/16W,5% ,0603,SMT	R7
271071105101	RES;1M ,1/16W,1% ,0603,SMT	PR123
271071105301	RES;1M ,1/16W,5% ,0603,SMT	R16,R39
271071106301	RES;10M ,1/16W,5% ,0603,SMT	R312

9. Spare Parts List

Spare Part List 3

Part Number	Description	Location(S)
271071107311	RES;107K ,1/16W,1% ,0603,SMT	PR103
271071125301	RES;1.2M ,1/16W,5% ,0603,SMT	PR29
271071131101	RES;130 ,1/16W,1% ,0603,SMT	R14A
271071140101	RES;14 ,1/16W,1% ,0603,SMT	R132
271071147011	RES;147 ,1/16W,1% ,0603,SMT	R71
271071162211	RES;16.2K,1/16W,1% ,0603,SMT	PR42
271071169011	RES;169 ,1/16W,1% ,0603,SMT	R137,R54
271071169311	RES;169K ,1/16W,1% ,0603,SMT	PR109
271071182214	RES;18.2K,1/16W,1%,0603,SMT	PR147
271071183101	RES;18K ,1/16W,1% ,0603,SMT	PR144
271071201101	RES;200 ,1/16W,1% ,0603,SMT	R228,R231
271071202301	RES;2K ,1/16W,5% ,0603,SMT	R12
271071221311	RES;221K ,1/16W,1% ,0603,SMT	PR154
271071223302	RES;22K ,1/16W,5% ,0603,SMT	PR30
271071224301	RES;220K ,1/16W,5% ,0603,SMT	R41
271071270301	RES;27 ,1/16W,5% ,0603,SMT	R119
271071274211	RES;27.4K,1/16W,1% ,0603,SMT	PR39
271071287111	RES;2.87K,1/16W,1% ,0603,SMT	PR40
271071301311	RES;301K ,1/16W,1% ,0603,SMT	R13,R3
271071309211	RES;30.9K,1/16W,1% ,0603,SMT	PR127
271071324211	RES;32.4K,1/16W,1% ,0603,SMT	PR24,PR51,PR58,PR64
271071330302	RES;33 ,1/16W,5% ,0603,SMT	PR135
271071333301	RES;33K ,1/16W,5% ,0603,SMT	R2
271071390302	RES;39 ,1/16W,5% ,0603,SMT	R118
271071402311	RES;402K ,1/16W,1% ,0603,SMT	PR132
271071411102	RES;412,1/16W,1% ,0603,SMT	R283
271071422211	RES;42.2K,1/16W,1% ,0603,SMT	PR5
271071432111	RES;4.32K,1/16W,1% ,0603,SMT	R10
271071432211	RES;43.2K,1/16W,1% ,0603,SMT	R1
271071453211	RES;45.3K,1/16W,1% ,0603,SMT	PR83
271071472101	RES;4.7K ,1/16W,1% ,0603,SMT	PR133
271071474301	RES;470K ,1/16W,5% ,0603,SMT	PR134,PR31,PR45
271071475011	RES;475 ,1/16W,1% ,0603,SMT	PR33
271071475811	RES;47.5 ,1/16W,1% ,0603,SMT	PR41
271071499311	RES;499K ,1/16W,1% ,0603,SMT	PR119
271071549211	RES;54.9K,1/16W,1% ,0603,SMT	PR49
271071560101	RES;56 ,1/16W,1% ,0603,SMT	R233,R238,R259,R275
271071563101	RES;56K ,1/16W,1% ,0603,SMT	R6
271071604111	RES;6.04K,1/16W,1% ,0603,SMT	R72
271071619011	RES;619 ,1/16W,1% ,0603,SMT	PR23,PR26,PR28
271071634211	RES;63.4K,1/16W,1% ,0603,SMT	PR94
271071634311	RES;634K ,1/16W,1% ,0603,SMT	PR125
271071753301	RES;75K ,1/16W,5% ,0603,SMT	R8
271071806111	RES;8.06K,1/16W,1% ,0603,SMT	PR101,PR78
271071806211	RES;80.6K,1/16W,1% ,0603,SMT	PR27
271072474101	RES;470K ,1/10W,1% ,0603,SMT	R4,R5,R9
271586026101	RES;.02 ,2W,1%,2512,SMT	PR122,PR126
271611000301	RP;0*4 ,8P ,1/16W,5% ,0612,SMT	RP5
271611100301	RP;10*4 ,8P ,1/16W,5% ,0612,SMT	RP10,RP12,RP14,RP16,RP18,RP2
271611102301	RP;1K*4 ,8P ,1/16W,5% ,0612,SMT	RP2

9. Spare Parts List

Spare Part List 4

Part Number	Description	Location(S)
271611103301	RP;10K*4 ,8P ,1/16W,5% ,0612,SMT	RP1,RP24,RP27,RP3,RP39,RP40
271611330301	RP;33*4 ,8P ,1/16W,5% ,0612,SMT	RP11,RP13,RP15,RP17,RP19,RP2
271611750301	RP;75*4 ,8P ,1/16W,5% ,0612,SMT	RP4,RP7
271611822301	RP;8.2K*4,8P ,1/16W,5% ,0612,SMT	RP58,RP59,RP6,RP64
272001106705	CAP;10U,10V,+80-20%,0805,Y5V,SMT	C146,C159,C164,C185,C320
272002105701	CAP;1U ,CR,16V ,-20+80%,0805,Y5	PC29,PC46,PC61
272002225701	CAP;2.2U ,CR,16V ,+80-20%,0805,Y	PC38
272003105701	CAP;1U ,CR,25V ,+80%-20%,0805,	PC145,PC148,PC19
272005104401	CAP;.1U ,CR,50V,10%,0805,X7R,IN	PC37,PC51,PC53
272005104705	CAP ;1U CR 50V +80-20% 0805 Y5V	C17,C18
272011106404	CAP;10U,6.3V,10%,1206,X7R,SMT	C129,C29,C302,C318,C319,C32,
272011106701	CAP;10U ,10V,+80-20%,1206,Y5V,S	C100,C225,C274,C275,C279,C346
272011226401	CAP;22U,6.3V,+-20%,1206,X5R,SMT	C288
272012105401	CAP;1U ,CR,16V ,10%,1206,X7R,S	C14A,C14B
272023475401	CAP;4.7U ,25V ,10%,1210,X5R,SMT	C1
272030102301	CAP;100P,3KV,5%,1808,NPO,SMT,PWR	C20
272030102405	CAP;1000P,CR,3KV,10%,1808,X7R,TU	C2,C3,C41
272071105403	CAP;1U ,10V ,10%,0603,X5R,SMT	C10,C4
272071105701	CAP;1U ,CR,10V ,80-20%,0603,Y5	PC12,PC128,PC129,PC130,PC142
272071332401	CAP;.33U ,10V ,10%,0603,X7R,SMT	C2
272072104402	CAP;.1U ,CR,16V,10%,0603,X7R,SM	C12,C17,C6
272072393401	CAP;.039U,CR,16V ,10%,0603,X7R,S	PC13
272072683404	CAP;.068U ,16V ,10%,0603,X7R,SMT	C16
272073223401	CAP;.022U,CR,25V ,10%,0603,X7R,S	C9
272073472301	CAP;4700P,CR,50V ,5% ,0603,X7R,S	C15A

Part Number	Description	Location(S)
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	PC151,PC153,PC32,PC45,PC60
272075103401	CAP;.01U ,CR,50V ,10%,0603,X7R,S	C11,C13,C3,C8
272075103408	CAP ;0.1U CR 50V 10% 0603 X7R S	C15,C16,C35,C37,C38,C39
272075103706	CAP; 0.1U CR 50V +80-20% 0603 Y	C28,C30,C31,C32,C33,C34
272075104701	CAP;.1U ,50V,+80-20%,0603,Y5V,S	PC10,PC101,PC103,PC108,PC112
272075120301	CAP;12P ,CR,50V ,5% ,0603,NPO,S	C281,C282
272075152401	CAP;1500P,CR,50V,10%,0603,X7R,SM	PC110,PC81
272075181301	CAP;180P ,50V ,5% ,0603,NPO,SMT	PC74
272075220301	CAP;22P ,50V ,5% ,0603,COG,SMT	C143,C160,C195,C196,C217,C221
272075221401	CAP;220P ,CR,50V ,10%,0603,X7R,S	PC11
272075222401	CAP;2200P,50V ,10%,0603,X7R,SMT	C5
272075223702	CAP; 0.22U CR 50V +80-20% 0603	C29,C40,C41
272075471401	CAP;470P ,50V,10%,0603,X7R,SMT	C36
272075471409	CAP; 0.0047U CR 50V 10% 0603 X7	C19
272075479301	CAP;4.7P,50V,5%,0603,NPO,SMT	C44
272102104401	CAP;.1U ,CR,10V,10%,0402,X5R,SM	C501,C502,C503,C504,C505,C506
272102105701	CAP;1U ,CR,6.3V ,80-20%,0402,Y	C101,C110,C111,C112,C117,C118
272102153401	CAP;.015U ,CR,16V,10%,0402,X7R,S	PC89
272105100303	CAP;10P ,CR,50V ,5%,0402,NPO,SM	C189,C229,C264,C266,C30,C31,
272105101401	CAP;100P ,50V ,5%,0402,COG,SMT	C1,C108,C109,C57,PC109,PC116,
272105102408	CAP;1000P,CR,50V,10%,0402,X7R,SM	C107,C11,C131,C150,C173,C20,
272105103702	CAP;.01U ,50V,+80-20%,0402,SMT	C183,C184,C191,C193,C228,C237
272105104701	CAP;.1U ,16V,+80-20%,0402,SMT	C10,C102,C103,C104,C105,C106,
272105222301	CAP;220P ,50V ,5% ,0402,NPO,SMT	C35
272105222501	CAP;2200P,50V ,+/-20%,0402,X7R,S	C67

9. Spare Parts List

Spare Part List 5

Part Number	Description	Location(S)
272105271403	CAP;270P ,50V,+-10%,0402,X7R,SMT	C154,C157,C289,C316,C4,C5,C6,
272421225501	CAP;220U,TPE,4V,20%,7343,SMT	PC166
272431156501	CAP;150U,6.3V,TPE,20%,7343,SMT	PC165
272625220401	CP;22P*4 ,8P,50V ,10%,1206,NPO,S	CP1,CP2
272990100301	CAP;10P,3000V,+- 5%,NPO,SMT	C19
272993106001	CAP;10U,25V,2.2mm,X5R,KYOCERA,SM	PC105,PC120,PC121,PC125,PC13
273000130019	FERRITE CHIP;120OHM/100MHZ,1608,	L10,L11,L12,L13,L14,L2,L22,L2
273000130038	FERRITE CHIP;600OHM/100MHZ,1608,	L39,L45,L49,L62
273000130062	INDUCTOR;120nH,10%,0603,SMT	L23
273000130106	FERRITE CHIP;600OHM/100MHZ,.2A,1	
273000150013	FERRITE CHIP;120OHM/100MHZ,2012,	PL1,PL13,PL15,PL16,PL17,PL18
273000150106	INDUCTOR;4.7UH,10%,2012,30mA,SMT	L20,L21
273000150313	CHOKE COIL;90OHM/100MHZ,20%,2012	L15,L16,L17,L18,L24,L25,L33,L
273000150326	INDUCTOR;4R7,2012,15mA;SMT,MAG.L	
273000500095	CHOCK COIL;0.5UH.1.0mOHM,25%,30A	PL10,PL8,PL9
273000500096	CHOCK COIL;4.7UH.20mOHM,25%,4.5A	PL14
273000500111	CHOCK COIL;3UH,14mOHM,7.5A,10039	PL11,PL12
273000500115	CHOKE COIL;400uH MIN,120mΩ MAX;	L19
273000990012	INDUCTOR;10UH,CDRH127,SUMIDA,SMT	PL19
273000990031	INDUCTOR;10UH,CDRH127B,SUMIDA,SM	PT1
273001050028	XSFORMER;10/100 BASE,LF-H41S,SMT	U4
273001050127	XFMR;CI8.5,30T/2150T,300mH,SMT,o	T1
281101015001	IC;MP1015EM-Z,CCFL CTRL,TSSOP20,	U1
282574186002	IC;74AHCT1G86,SINGLE,XOR,SOT23,S	U14
283467540001	IC;EEPROM,M24C02-WMN6T,2K,SO8,SM	IC6

Part Number	Description	Location(S)
283467540002	IC;EEPROM,M93C46-WMN6T,64*16 BIT	U16
283467640002	IC;FLASH,256K*8, PLCC32, LPC, ST	
283468290001	IC;FLASH,256K*8,PLCC32,SST49LF02	
283468290002	IC;FLASH,256K*8,PLCC32,PM49FL002	
284500301004	IC;SIS301LV,TV ENCODER/LVDS,128P	U9
284500661001	IC;SISM661FX,N.B,BGA 839P	U12
284500781001	IC;G781,TEMPERATURE MTR,SO8	U8
284500963004	IC;SIS963L,S.B.,BGA 371P	U20
284501410007	IC;PCI1410A,PCI/CARDBUS,PQFP,144	U22
284501616002	IC;VT1616,6-CHANNEL CODEC WITH S	U11
284501883001	IC;ICS1883AF,LAN PHY,SMT,SSOP48	U5
284583950002	IC;W83L950D-Ver.C,LPC_KBC,LQFP,8	
284593772002	IC;ICS93772CF,DDR ZERO DELAY CLO	U19
284595200701	IC;ICS952007,CLOCK GEN,SSOP,48P	U13
286100358001	IC;LMV358M,DUAL AMP.,LOW VOLT.,S	PU2
286100393004	IC;LMV393,DUAL COMPARTOR,SSOP,8P	PU21
286101422001	IC;G1422,AMPLIFIER,2W,TSSOP,20P,	U10
286300431014	IC;SC431LCSK-.5,.5%,ADJ REG,SOT2	PQ40
286301414001	IC;MM1414,PROTECTION,TSOP-20A,PR	IC7
286301772001	IC;MAX1772,PWM,QSOP,28P	PU22
286302211001	IC;TPS2211,POWER DISTRI SW,SSOP1	U21
286302211004	IC;TPS2211A,POWER INTERFACE SW,S	
286302951015	IC;LP2951ACM,VOLTAGE REGULATOR,S	PU3
286302996001	IC;G2996,DDR,GMT,SOP8FD,SMT	PU8
286303728002	IC;LTC3728LX,PWM CTRL,LTC,5X5 QF	PU11,PU14

9. Spare Parts List

Spare Part List 6

Part Number	Description	Location(S)
286304377001	IC; MAX4377F,I-SENSEAMP ,MSOP8,S	PU20
286306207001	IC;ISL6207CB,PWM DRIVER,SO8,SMT	PU5,PU6,PU7
286306247001	IC;ISL6247,PWM CONTROLLER,40-QFN	PU1
286307805019	IC;AZ78L05,VOL REGULATOR,SOT-89,	U15
286308800006	IC;AME8800AEEV,VOL REG.,SOT23-5,	PU4
286309181002	IC;RT9181, 150mA LDO with POG,SO	U3
286309701001	IC;RT9701,POWER DISTRI SW,SOT23-	U1,U2,U7
286317812001	IC;HA178L12UA,VOLT REGULATOR,SC-	PU17
286369229301	IC;G692L293T,RESET CIRCUIT,2.93V	U18
286387506001	IC;S-875061EUP VOLT DETECTOR S	IC5
288100024004	DIODE;ZMD24,ZENER,24V,1W,5%,SMT	PD4
288100032013	DIODE;BAS32L,VRRM75V,MELF,SOD-80	PD8
288100056003	DIODE;BAW56,70V,215mA,SOT-23	PD16
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	ZD3,ZD4
288100056005	DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM	PD2
288100070006	DIODE;BAV70LT1,70V,225MW,SOT-23,	
288100112003	DIODE;EC11FS2-TE12L,SCHOTTKY,200	PD14
288100541002	DIODE;BAT54ALT1,COM. ANODE,SOT-2	D33,PD11,PD13
288100701002	DIODE;BAV70LT1,70V,225MW,SOT-23	D15,PD1,PD3
288100840001	DIODE;SM840B,40V,8A,STD-202	PD5,PD7
288101004024	DIODE;EC10QS04,RECT,40V,1A,CHIP,	PD12
288103104001	DIODE;EC31QS04-TE12L,40V,3A,SMT	PD10,PD6,PD9
288104148001	DIODE;RLS4148,200MA,500MW,MELF,S	D19,D20,D21
288110355001	DIODE;1SS355,80V,100mA,SOD-23,SM	D3
288111544001	DIODE; 1SR-154-400 400V 1.0A	D4

Part Number	Description	Location(S)
288200144001	TRANS;DTC144WK,NPN,SOT-23,SMT	PQ12,PQ35
288200144003	TRANS;DTC144TKA,N-MOSFET,SOT-23	PQ18,Q10,Q14,Q22,Q23,Q26,Q29
288200144008	TRANS;DTA144EKA,PNP,SMT	Q8
288200610001	TRANS;TP0610T,P-MOSFET,SOT-23	PQ9
288200717001	DIODE;RB717F,SCHOTTKY,40V,SOT323	SD2
288202240001	TRANS;MUN2240T1,NPN,SOT-23,ON	
288203400001	TRANS;AO3400,N-MOSFET,SOT-23	PQ26,PQ30,Q4
288203401001	TRANS;AO3401,P-MOSFET,SOT-23	PQ13,PQ17,PQ34
288203403001	TRANS;AO3403,P-MOSFET,SOT-23,ALP	Q8,Q9
288203904010	TRANS;MMBT3904L,NPN,Tr35NS,TO236	PQ6,Q13,Q17,Q21,Q31,Q34
288203906018	TRANS;MMBT3906L,PNP,Tr35NS,TO236	Q30
288204407001	TRANS;AO4407,P-MOS,.01OHM,SO8,SM	PQ38,PQ39,PQ7,PQ8
288204409001	TRANS;AO4409,P-MOSFET,SO-8P,MSL,	Q10,Q14
288204410010	TRANS;AO4410,N-MOSFET,ID=18A,0.0	PU10
288204422001	TRANS;AO4422,24mOHM,N-MOSFET,SOI	PU13,PU19
288204800001	TRANS;SI4800DY,N-MOS,.0185OHM,SO	PU16
288204814001	TRANS;SI4814,26.5mOHM,N_MOS ,SMT	PU15,PU23,PU9
288204832001	TRANS;SI4832DY,N-MOSFET,.028OHM,	PU18
288204892001	TRANS;SI4892DY,N-MOSFET,SO8	PU12
288205003004	TRANS;SUD50N03-11,N-MOS,TO252	PQ15,PQ16,PQ20,PQ21,PQ23,PQ
288206035005	TRANS;FDD6035AL,46A,30V,16mOHM,T	PQ14,PQ19,PQ22
288206405001	TRANS;AO6405,87mOHM ,P-MOS,SMT	PQ42,PQ43
288227002001	TRANS;2N7002LT1,N-CHANNEL FET,SO	PQ1,PQ10,PQ11,PQ2,PQ27,PQ28
291000000203	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	J2
291000000708	CON;BATTERY,7P,FM,2.5MM,BTG-07AR	CON1

9. Spare Parts List

Spare Part List 7

Part Number	Description	Location(S)
291000001206	CON;MINI PCI SOCKET,P124,QTC,C10	
291000010209	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	
291000010410	BFM-SC,CON;HDR,MA,4P*1,1.25MM,ST	
291000013016	CON;HDR,MA,15P*2,1MM,H4.25,ST,SM	J6
291000020204	CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM	
291000020222	CON;HDR,MA,2P*1,1.25MM,H4.2,ST,S	J10,J12,J19,J5
291000020415	CON;HDR,MA,4P*1,1.25MM,ST,SMT,38	J8
291000143011	CON;FPC/FFC,15P*2,.8MM,BD/BD,ST,	J15
291000150606	CON;FPC/FFC,6P,0.5MM,R/A,SMT	J20
291000150607	CON;FPC/FFC,6P,0.5MM,R/A,SMT,200	
291000152610	CON;FPC/FFC,26P,1MM,H=2.0,R/A,85	
291000152614	CON;FPC/FFC,26P,1MM,H=2.0,R/A,SM	J501
291000611255	MINIPCI SOCKET;124P,0.8MM,H=9.2,	J13
291000614795	IC SOCKET;BGA-mPGA478B,478P,AMP	U6
291000616805	CON;PCMCIA CARD,68P,TAI-SOL,246-	J502
291000811001	CON;PHONE JACK,10P,R/A,RJ45,RJ11	J7
291000811011	CON;PHONE JACK,10P,R/A,RJ45,RJ11	
291000923002	CON;MDC,15P*2,.8MM,BD/BD,ST,SMT,	
294011200016	LED;GREEN,H0.8,0603,CL-190G,SMT	D501,D502,D503,D504,D505,D50
294011200200	LED;GREEN/RED,H0.8,W1.9,19-22SRV	D509
295000010116	FUSE;FAST, 10A, 86VDC, 6125,SMT	PF1,PF2
295000010154	FUSE;FAST,1.25A,63V,1206,SMT,043	F1
297030100015	SW;TOGGLE,SPST,5V/1mA,4P,SMT,TAI	SW506
297030105003	SW;TOGGLE,SPST,5V/1mA,MPU-101-80	
297040100027	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	

Part Number	Description	Location(S)
297040105010	SW;PUSH BUTTOM,5P,SPST,12V/50MA,	SW501,SW502,SW503,SW504,SW
310111103013	THERMISTOR;10K,1%,RA,DISK,103AT-	RT2
310111103025	THERMISTOR;10K,1%,RA,DISK,103AT-	
310111103031	THERMISTOR;10K,1%,150MM,BN35-3H1	
312271006358	EC;100U,25V,RA,M,D6.3*7,SGX,SANY	PC159,PC160,PC63,PC64
312272205359	EC;22U ,20V,20%,RA,D6.3*5,OS-CO	PC25,PC26,PC58
312272206101	EC;220U ,6.3V,M,6.3*5,-55+105',D	C12,C13,C136,C14,C15,C170,C52
312272206102	EC;220U ,10V,M,6.3*9,-55+105',DI	
312273361501	EC;330U ,6.3V ,RA,M,6.3*7,+105C	
312276806151	EC;680U ,6.3V,20%,D10,105'C,OS-C	PC127
312276806158	EC;680U,6.3V,20%,RA,10*10.5,105	
312278206151	EC;820U ,4V,+-20%,100*10.5,SP.OS	PC72,PC95
312278206161	EC;820U ,2.5V,+-20%,8X12.5,OS-CO	PC41,PC42,PC49,PC50,PC56,PC5
314100143505	XTAL;14.31818MHZ,30PPM,32PF,49S,	X3
314100143506	XTAL;14.31818MHZ,30PPM,32PF,AT49	
314100245504	XTAL;24.576MHZ,30PPM,16PF,49S,11	X2
314100250502	XTAL;25MHZ,30PPM,20PF,49S,11.5*3	X1,X6
314100327214	XTAL;32.768KHZ,12.5PF,20PPM,3*8,	X7
314149800402	XTAL;8MHZ,30PPM,HC-49/S,6B080002	X4
316678100001	PCB;PWA-INVERTER BD (DA-1A10-A);	R0C
316682900001	PCB;PWA-8599/M BD	R06
316682900003	PCB;PWA-8599/BATT ,PR AND GA BD	
323768290002	DDR SDRAM MODULE;256MB,184PIN,DD	
324180786744	IC;CPU,Celeron,2.8G,FSB 400,MICR	
331000000083	CON;HOLDER,PCMCIA,TAI-SOL,246-00	

9. Spare Parts List

Spare Part List 8

Part Number	Description	Location(S)
331000007038	CON;BAT,7P,2.5mm,OCT,tBTD-007001	PJ2
331000007044	CON;BAT,7P,2.5mm,ALLTOP,C10368	
331000008090	CON;USB,MA,ST,4P*2,SMT,020122MR0	
331000008091	CON;USB,MA,ST,4P*2,SMT,1-1470748	J3,J4,J9
331000050004	CON;CD-ROM,50P,0.8MM,H-10.4,R/A,	J21
331000050005	CON;CD-ROM,50P,0.8MM,H-10.4,R/A,	
331030044021	CON;HDR,FM,22P*2,2.0MM,SMT,C1783	J16
331030044023	CON;HDR,FM,22P*2,2.0MM,SMT,2001	
331650047804	IC SOCKET;BGA-PGA478B-SKT,MOLEX,	
331660018441	DIMM SOCKET;DOUBLE STACK DDR,202	J18
331678100001	CONNECTOR;7 PIN,1.25mm,SMT,ACES,	J1
331720015071	CON;D,FM,15P,2.29,R/A,SUYIN	J2
331840005013	CON;STEREO JACK,5P,R/A,28MF60-07	J11
331840005014	CON;STEREO JACK,5P,R/A,28MF60-05	J14
331870007010	CON;MINI DIN,7P,R/A,W/GROUND,030	J1
331910002006	CON;POWER JACK,2P,20VDC,5A,DIP	PJ1
332110020027	WIRE;#20,UL1007,50MM,BLACK,PRC	VL-VL
332110020097	WIRE;#20,UL1007,74MM,BLACK,YIYI;	
332110020175	WIRE;#20,UL1007,L=103MM,RED, PWR	CN10
332110026097	WIRE;#26,UL1007,55MM,BLACK,PRC	
332110026155	WIRE;26#,UL1061,L=115MM,YELLOW,	CN9
332110026156	WIRE;#26,UL1061,L=136.5MM,WHITE,	CN8
332810000197	PWR CORD;125V/7A,3P,BLACK,AMERIC	
333020000008	SHRINK TUBE;600V,125℃,Φ2.5mm,L	
333025000004	SHRINK TUBE;300V,125,I.D=2.5,T=0	

Part Number	Description	Location(S)
333050000120	SHRINK TUBE;600V,105'C,D0.8*9MM,	
335152000044	CFM-BAT;FUSE THERMAL 98'C	
335152000085	FUSE; 128 DC-7A/50V 139℃only UC	F2
335152000094	FUSE;LR4-900,POLY SWITCH	
335152000100	FUSE; THERMAL,SF91E-1/94℃,10A/2	
338536010006	BATTERY;LI,3.6V/2.0AH,18650,PANA	
339115000046	MICROPHONE;-62dB+-2dB,D6.0*H2.7,	MIC501
339115000059	MICROPHONE;-44dB+-3dB,D6.0*H5.0,	
339115000060	MICROPHONE; -62+/-3dB,60*27mm;HO	
340682900001	HOUSING ASSY;LCD,8599	
340682900002	COVER ASSY;LCD,8599	
340682900003	HINGE;R,8599	
340682900004	HINGE;L,8599	
340682900005	HINGE;R,SZS,8599	
340682900006	HINGE;L,SZS,8599	
340682900007	COVER ASSY;TOP,8599	
340682900009	BRACKET ASSY;TOUCH-PAD,8599	
340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHI	
340682900011	SPEAKER ASSY; 28*4.3,2W,VECO,859	
340682900013	HEATSINK ASSY;CPU,NORTHWOOD,MPT,	
340682900014	HEATSINK ASSY;CPU,NORTHWOOD,ALRO	
340682900015	HOUSING ASSY;BOTTOM,8599	
340682900016	SHIELDING ASSY;BOTTOM,8599	
340682900017	COVER ASSY;CPU,8599	
340682900018	COVER ASSY;MINIPCI,8599	

9. Spare Parts List

Spare Part List 9

Part Number	Description	Location(S)
340682900019	HAETSINK ASSY;SYSTEM,M/B,MPT,859	
340682900020	HAETSINK ASSY;SYSTEM,M/B,ALRO,85	
340682900021	SHIELDING ASSY;HDD,8599	
340682900023	COMBO BEZEL ASSY; QSI,SBW-242B,8	
341682900003	BRACKET;LCD,R,8599	
341682900004	BRACKET;LCD,L,8599	
342502900001	CONTACT PLATE;W4L27T0.15,7068	
342503200003	CONTACT PLATE;W4L18T0.15,7521/GR	
342503400005	CONTACT PLATE;W5L24T0.13,7170LI,	
342682900009	BRACKET;ROM,8599	
342682900010	CONTACT PLATE;W5L28T0.15MM,BATTE	
342682900011	CONTACT PLATE;W5L37.75T0.15MM,1/	
342682900012	CONTACT PLATE;W4L18.5T0.15MM,1/2	
342682900015	FINGER;EMI SMD FINGER,H=5.5,8599	
344672300025	DUMMY CARD;PCMCIA,MANGUSTA	
344682900012	COVER;HINGE,8599	
344682900016	COVER;BATTERY,8599	
344682900017	HOUSING;BATTERY,8599	
345668900016	SPONGE;BIOS BATT,M722	
345675400023	RUBBER;DOWN LCD,8355	
345682900005	SPONGE;DUAL DDR,M/B,8599	
345682900006	SPONGE;SPSPEND SWITCH,M/B,8599	
345682900009	SPONGE;HINGE COVER,8599	
345682900013	INSULATOR;S-VIDEO,M/B,8599	
345684500004	RUBBER;SYSTEM HEATSINK,TARZAN	

Part Number	Description	Location(S)
346502800004	INSULATOR;BATT ASSY,BATT+,BATT-,	
346503100001	INSULATOR;BATT ASSY,THERMAL FUSE	
346503100005	INSULATOR;5,BATTERY ASSY,7521Li	
346503200202	INSULATOR;BATT ASSY,ONE ROUND,BL	
346503400503	INSULATOR;BATT ASSY,W7L13,8175	
346673420003	MYLAR;15*10*0.8,8640P	
346677300001	INSULATOR;FIBER,UL94V-0,D=17.5mm	
346678600005	INSULATOR;FIBER,UL94V-0,64X15,T=	
346682900005	INSULATOR;CARD BUS,8599	
346682900006	INSULATOR;SOUTH BRIDGE,8599	
346682900007	NYLON;BATTERY PULL,8599	
346682900009	AL-FOIL;T/P BRACKET,8599	
346682900010	AL-FOIL;T/P SWITCH,MB,8599	
346682900013	SPONGE;M/B,8599	
346682900014	INSULATOR;AL-FOIL,INVERTER,8599	
346684400001	INSULATOR;RIBRE,101*15*0.25MM,BA	
346684400002	INSULATOR;RIBRE,63*15*0.25MM,BAT	
347104030012	GASKET;1,04,030,012	
347104030030	GASKET;1,04,030,030	
347104045125	GASKET;1,04,045,125	
347105020090	GASKET;1,05,020,090	
347105060030	GASKET;1,05,060,030	
347105060060	GASKET;1,05,060,060	
347108010012	GASKET;1,08,010,012	
347108080090	GASKET;1,08,080,090	

9. Spare Parts List

Spare Part List 10

Part Number	Description	Location(S)
347108150024	GASKET;1,08,150,024	
347110020025	GASKET;1,10,020,025	
347110035035	GASKET;1,10,035,035	
347110040012	GASKET;1,10,040,012	
347110080025	GASKET;1,10,080,025	
361200001018	CLEANNER;YC-336,LIQUID,STENCIL/P	
361200003047	SOLDER PASTE;NO CLEAN,RMA,CK3000	
361400003005	ADHESIVE;HEAT,TRANSFER,HTA-48(W)	
361400003030	ADHESIVE;ABS+PC PACK,G485,CEMIDA	
361400003037	SOLDER CREAM;SH-6309,SHENMAO,63/	
370102010205	SPC-SCREW;M2L2(t0.3),N/W/WLK	
370102010256	SPC-SCREW;M2L2.5,K-HD(t0.5) NLK,	
370102610603	SPC-SCREW;M2.6L6,K-HD,NIB/NLK	
370103010405	SPC-SCREW;M3L4,NIW,K-HD,T0.3	
370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,	
370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYL	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,N	
371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	
371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	
371102610308	SCREW;M2.6L3,D3.5,t=0.5,K-HD,NIW	
371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	
371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	
373101712351	T-SCREW;B,M1.7,L2.35,K-HD,2,NIB	
377102650901	S-STANDOFF;M2.6DP3.5H9L1.1,NIW	MTG2,MTG3

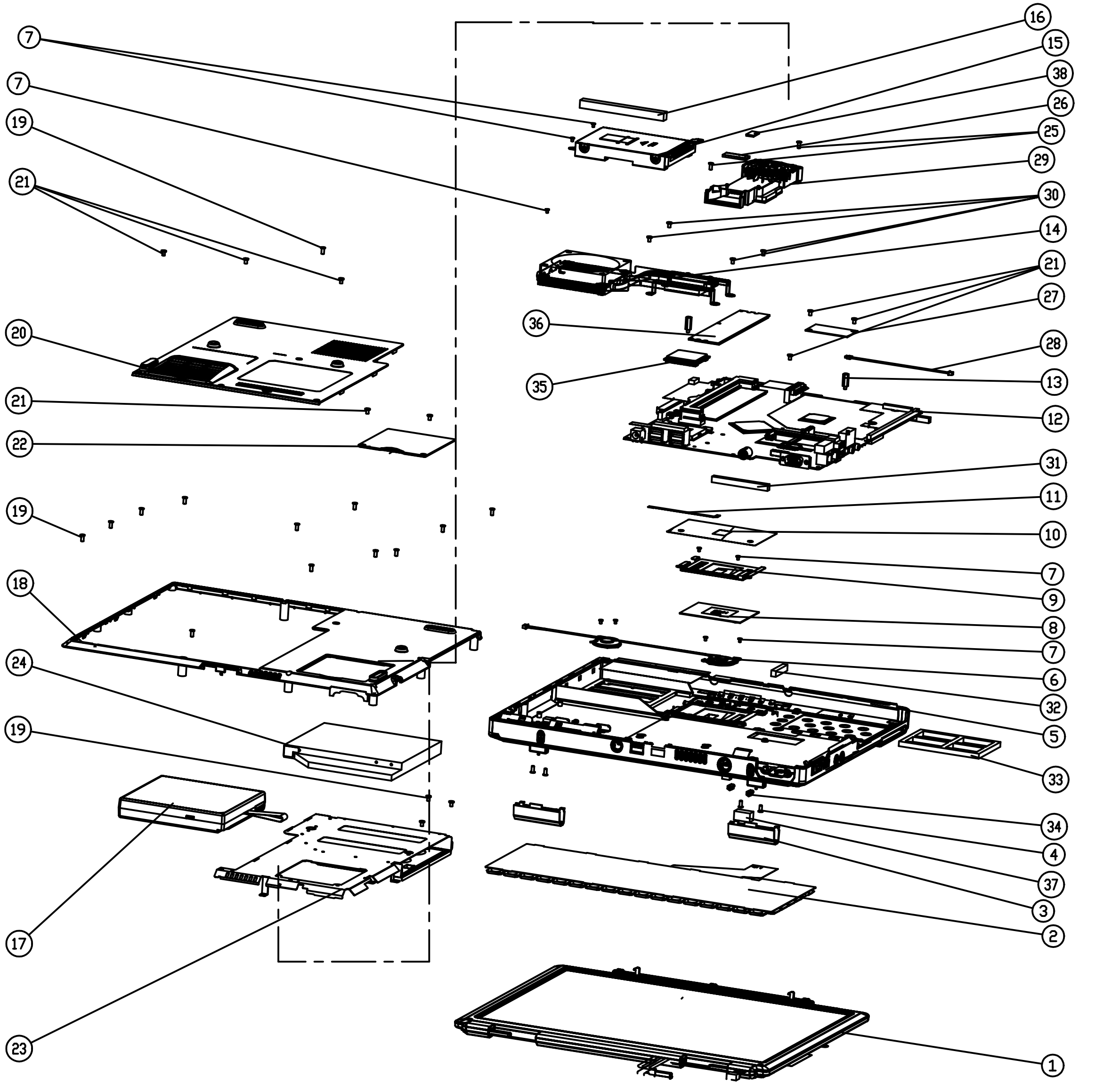
Part Number	Description	Location(S)
377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NY	
377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	
411678100001	PWA;PWA-INVERTER BD,DA-1A10-A,PW	
411678100002	PWA;PWA-INVERTER BD,SMT,DA-1A10-	
411682900001	PWA;PWA-8599,MOTHER BD	
411682900002	PWA;PWA-8599,MOTHER BD,T/U	
411682900003	PWA;PWA-8599,MOTHER BD,SMT	
411684410001	PWA;PWA-BATT,PCB BD,LI,4.0Ah,2P4	
411684410002	PWA;PWA-BATT,BATT BD,SMT,BL-4240	
412678800001	PCB ASSY;FAX MODEM 56K,1456VQL4A	
413000020386	LCD;HSD150PX14-A,TFT15",XGA,HANN	
416268290011	LT PF;HANNSTAR,XGA,HSD150PX14-A,	
421311310001	CABLE ASSY;PHONE LINE,6P2C,W/Z C	
421675400012	WIRE ASSY;BIOS,BATTERY,8355	
421676400001	WIRE ASSY,MDC-MODEM,APOLLON	
421682900004	WIRE ASSY;HSD150PX14-A,8599	
421682900007	WIRE ASSY;ANTENNA,8599	
421682900014	WIRE ASSY;HSD150PX14-A,GREATLAND	
422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,859	
422682900002	FFC ASSY;TOUCH-PAD,HONG-FU,8599	
422682900003	FFC ASSY;TOUCH-PAD,CEI,8599	
431682900001	CASE KIT;ID1,256KB 8599	
441682900010	LCD ASSY;HANNSTAR,XGA,HSD150PX14	
441684410001	BATT ASSY;14.8V,4.0Ah,LI,BL-424	
441684410002	BATT ASSY;14.8V,4.0Ah,LI,BL-424	

9. Spare Parts List

Spare Part List 11

Part Number	Description	Location(S)
441684410004	BATT ASSY;14.8V,4.0Ah,LI,CASE CL	
441684410005	BATT ASSY;14.8V,4.0Ah,LI,CORE PA	
441684410006	CONTACT PLATE ASSY;W5L45T0.13,FU	
441684410007	CONTACT PLATE ASSY;PTC,S-TUBE,BL	
441999900330	BATT ASSY OPTION;LI,8-CELL,ID1,8	
442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PU	
442682900021	AC ADPT ASSY;19V,6.32A,DELTA ADP	
451682900001	HDD ME KIT;8599	
451682900003	LCD ME KIT;15",XGA,Hannstar,8599	
451682900005	ROM ME KIT;8599	
451682900006	LABEL KIT;N-B,w/o Intel Inside L	
451682900007	HOUSING KIT;8599	
461677400001	PACKING KIT;DA-1A05-A;PWR	
461682900002	PACKING KIT;COMPACT,N-B,8599	
481682900001	F/W ASSY;SYS/VGA BIOS,8599	U23
481682900002	F/W ASSY;KBD CTRL,8599	U17
523402379051	HDD DRIVE;40GB,2.5",MHT2040AT,V4	
523430061010	DVD COMBO DRIVE;24X10X8X24,SBW-2	
523468290002	COMBO ASSY;SBW-242B,8599	
523468290005	HDD ASSY;FUJITSU,MHS2040AT,8599	
526268290006	LTXNX;8599/5RYB/40C/1UI9/A1D2A/X	
531010570032	KBD;88,UI,5035,BTC,8599	
561568290002	MANUAL;QSG,EN,8599	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	

Part Number	Description	Location(S)
600100010009	SOLDER WIRE;63/37,0.8,CM,N/C,PRC	
624200010140	LABEL;5*20,BLANK,COMMON	
624200010140	LABEL;5*20,BLANK,COMMON	



SCALE 0.200

ITEM	PaRT NO	PART NAME	Q'TY	TYPE	MARK
38	345684500004	RUBBER;SYSTEM HEATSINK,TARZAN	1	part	
37	345682900009	SPONGE;HINGE COVER,8599	1	part	
36	323768290001	DDR SDRAM MODULE ;512MB,184PIN,DDR400,77.103736.464,APACER	1	part	OPTION
35	324180786587	IC;CPU,P4-NORTHWOOD,3.06G,FSB 533,MICRO_FCPGA,478P	1	part	OPTION
34	377244010002	STANDOFF;#4-40DP3.5H5L5.5,NIW	2	part	
33	344672300025	DUMMY CARD;PCMCIA,MANGUSTA	1	part	
32	347105060030	GASKET;1,05,060,030	1	part	
31	347105060060	GASKET;1,05,060,060	1	part	
30	370103010414	SPC-SCREW;M3L4,KHD,NIW/NLK,D5.3,t0.8	4	part	
29	340682900019	HAETSINK ASSY;SYSTEM,M/B,MPT,8599	1	asm	OPTION
28	421676400001	WIRE ASSY,MDC-MODEM,APOLLON	1	asm	
27	412155600047	PCB ASSY;MDM,56K,UNIV,F-PACK,WO/KIT	1	asm	
26	347110020025	GASKET;1,10,020,025	1	part	
25	371102010610	SCREW;M2L6,K-HD(+),t0.75,NIB	2	part	
24	523468290001	DVD+RW ASSY;SDW-041,8599	1	asm	OPTION
23	340682900016	SHIELDING ASSY;BOTTOM,8599	1	asm	
22	340682900018	COVER ASSY;MINIPCI,8599	1	asm	
21	371102610406	SCREW;M2.6L4,K-HEAD(+),NIB	8	part	
20	340682900017	COVER ASSY;CPU,8599	1	asm	
19	371102610607	SCREW;M2.6L6,K-HEAD(+),NIB	16	part	
18	340682900015	HOUSING ASSY;BOTTOM,8599	1	asm	
17	441999900321	BATT ASSY OPTION;LI,8-CELL,8599	1	asm	OPTION
16	347108080090	GASKET;1,08,080,090	1	part	
15	523468290004	HDD ASSY;HITACHI,IC25N040ATMR04,8599	1	asm	OPTION
14	340682900013	HEATSINK ASSY;CPU,NORTHWOOD,MPT,8599	1	asm	OPTION
13	377102651002	S-STANDOFF;M2.6DP5H12.5L4,NIW,NYLOK	2	part	
12	411682900001	PWA;PWA-8599,MOTHER BD (A)	1	asm	OPTION
11	422682900001	FFC ASSY;TOUCH-PAD,TENN-RICH,8599	1	asm	OPTION
10	346682900009	AL-FOIL;T/P BRACKET,8599	1	part	
9	340682900009	BRACKET ASSY;TOUCH-PAD,8599	1	asm	
8	442680900051	TOUCHPAD MODULE;SYNAPTICS,TM42PUM1950	1	part	
7	371102010310	SCREW;M2L3,K-HD(+),D3.8,t=0.75,NIW	9	part	
6	340682900010	SPEAKER ASSY; 28*4.3,2W,FENG-CHIUN,8599	1	asm	OPTION
5	340682900007	COVER ASSY;TOP,8599	1	asm	
4	370103010604	SPC-SCREW;M3L6,NIB,K-HD,t0.8,NYLOK	4	part	
3	344682900012	COVER;HINGE,8599	2	part	
2	531020237940	KBD;88,UI,K080818G1,8599	1	part	OPTION
1	441682900002	LCD ASSY;15",XGA,SAMSUNG,8599	1	asm	OPTION

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ITEM	CONTENTS OF CHANGE	RVS	CHK	APV	M/D/Y

TOL± RANGE	Pla	Met	Ins	Por	Cab	Pac	Gas	PCB
0~6	0.1	0.1	0.1	0.2	0.5	1	0.5	0.1
6~30	0.1	0.1	.15	.25	1	1	0.5	0.1
30~80	0.1	.15	0.2	0.3	2	1.5	1	0.1
80~180	.15	.15	.25	0.3	2	2	1	.15
180~315	.15	0.2	0.3	0.4	2.5	2	1	.15
315~800	0.2	0.3	0.4	0.5	3	3	2	.15

DATE	24-03-04	MATERIAL	SEE NOTES	TREATMENT		REMARK	
UNIT	MM	SCALE	0.2	DRAWING NAME	LT PF;15",XGA,SAMSUNG,8599		
DRAWN	DESIGNED	CHECKED	APPROVED	MATERIAL NO.	AD	416268290001	R00

MiTAC Technology Corp.

SHEET NO. 1 OF 1

model name8599_MAIN_ASSY

file nameDRW_8599_MAIN_ASSY

MODEL : 8599

Revision 06

Contexts

Title	Page
COVER SHEET & SCREW HOLE	1
System Block Diagram	2
Power Block Diagram	3
Prescott/Northwood (1/2)	4
Prescott/Northwood (2/2)	5
SIS M661FX(1/2)	6
SIS M661FX(2/2)	7
TV/LVDS ENCODER(SiS301LV)	8
DDR DIMMs	9
LCD&VGA Interface	10
Clock Generator/Buffer	11
SIS963L (1/3)	12
SIS963L (2/3)	13
SIS963L (3/3)	14
IDE Interface	15
PCMCIA (Ti PCI1410A)	16
LAN PHY (ICS1883AF) & MDC	17
USB 2.0 & Flash ROM	18
AUDIO CODEC	19
KBC (W83L950D)	20
MiNi-PCI & USB 2.0	21
Charge board	22
DC Connector	23
Battery Connector	24
+5V,+3V,+1.8V,+1.5V	25
+2.5V,1.25V,1.8VS	26
CPU_CORE1	27
CPU_CORE2	28
	29
	30
	31
	32
	33
	34

POWER STATES

STATE / SIGNAL	VOTAGE	POWER ON	STR	STD	MEC-OFF	REMARK
H8_SUSB	-	HIGH	LOW	LOW	LOW	
H8_SUSC	-	HIGH	HIGH	LOW	LOW	
ADP	+19V	O	O	O	O	
BATTERY	+12V	O	O	O	O	
+VCC_CORE	+1.75V	O	X	X	X	
+12V	+12V	O	O	X	X	
+12VS	+12V	O	X	X	X	
+5V	+5V	O	O	X	X	
+5VS	+5V	O	X	X	X	
+3V	+3.3V	O	O	X	X	
+3VS	+3.3V	O	X	X	X	
+2.5V_DDR	+2.5V	O	O	X	X	
+1.8V	+1.8V	O	O	X	X	
+1.8VS	+1.8V	O	X	X	X	
+1.25VS_DDR	+1.25V	O	X	X	X	
+5VA	+5V	O	O	O	O	
+3VA	+3.3V	O	O	O	O	
+3VAS	+3.3V	O	O	O	X	

IDSEL

IDSEL	CHIP
AD11	SiS 963
AD12	PCI to PCI Bridge
AD13	AC'97 Codec
AD14	USB
AD15	MII
AD20	Ti PCI1410A
AD21	MiniPCI

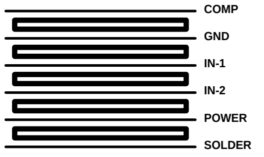
BUS MASTER

REQ/GNT	CHIP
-REQ0/-GNT0	Ti PCI1410
-REQ2/-GNT2	MINI PCI

PCIINT

PCIINT	CHIP
INTA#	SiS 301LV
INTB#	PCMCIA (PCI1410A)
INTC#	MINI PCI
INTD#	MINI PCI

Board Stackup-up



DRAW	DESIGN	CHECK	ISSUED

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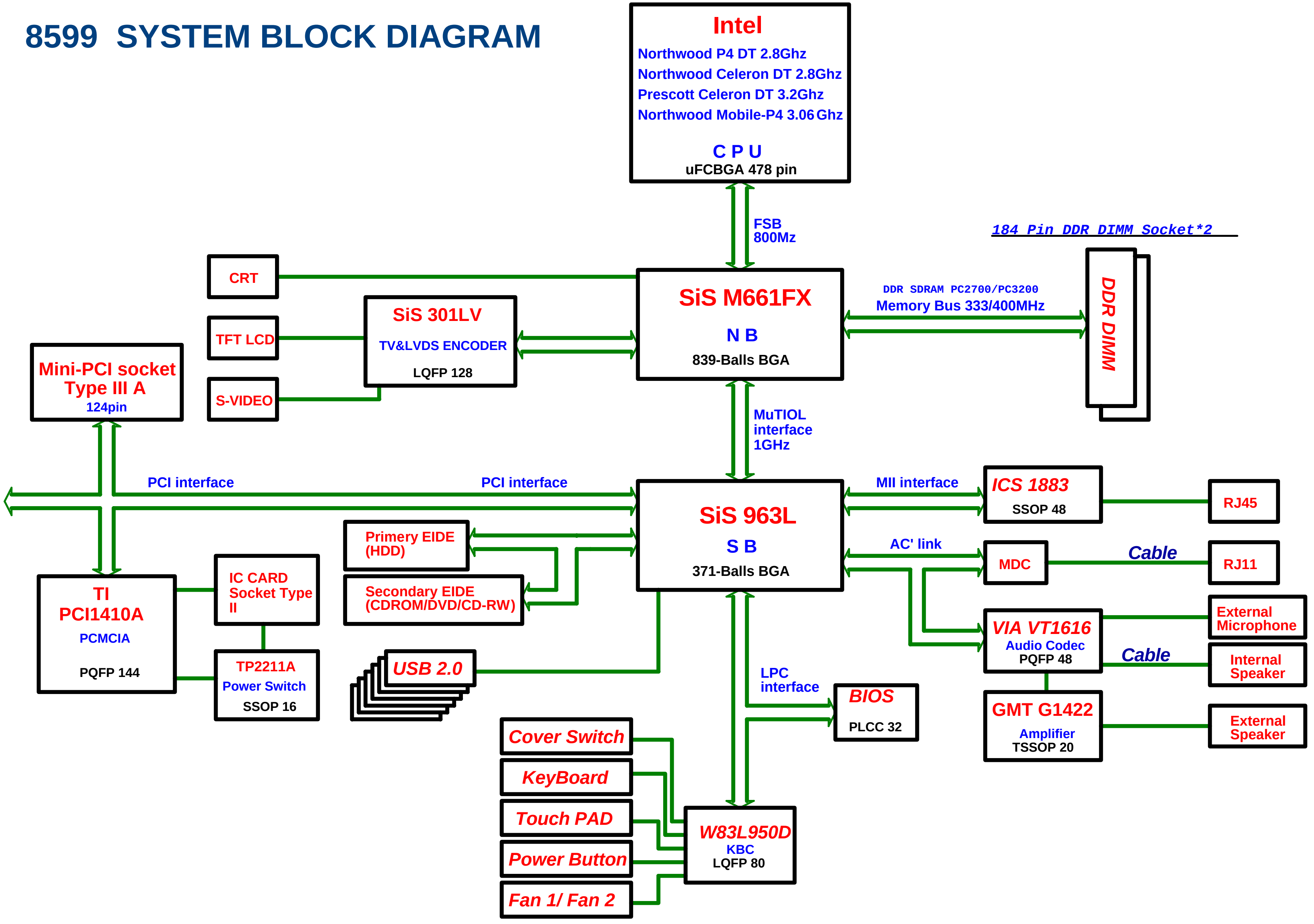
Title
COVER SHEET

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 1 of 28

8599 SYSTEM BLOCK DIAGRAM


Intel
Northwood P4 DT 2.8Ghz
Northwood Celeron DT 2.8Ghz
Prescott Celeron DT 3.2Ghz
Northwood Mobile-P4 3.06 Ghz
C P U
uFCBGA 478 pin
FSB
800Mz
184 Pin DDR DIMM Socket*2
DDR SDRAM PC2700/PC3200
Memory Bus 333/400MHz
DDR DIMM
SiS M661FX
N B
839-Balls BGA
CRT
TFT LCD
S-VIDEO
SiS 301LV
TV&LVDS ENCODER
LQFP 128
Mini-PCI socket
Type III A
124pin
MuTIOL
interface
1GHz
PCI interface
PCI interface
MII interface
ICS 1883
SSOP 48
RJ45
SiS 963L
S B
371-Balls BGA
Primery EIDE
(HDD)
Secondary EIDE
(CDROM/DVD/CD-RW)
AC' link
MDC
Cable
RJ11
TI
PCI1410A
PCMCIA
PQFP 144
IC CARD
Socket Type
II
TP2211A
Power Switch
SSOP 16
USB 2.0
VIA VT1616
Audio Codec
PQFP 48
External
Microphone
Cable
Internal
Speaker
LPC
interface
BIOS
PLCC 32
GMT G1422
Amplifier
TSSOP 20
External
Speaker
Cover Switch
KeyBoard
Touch PAD
Power Button
Fan 1/ Fan 2
W83L950D
KBC
LQFP 80

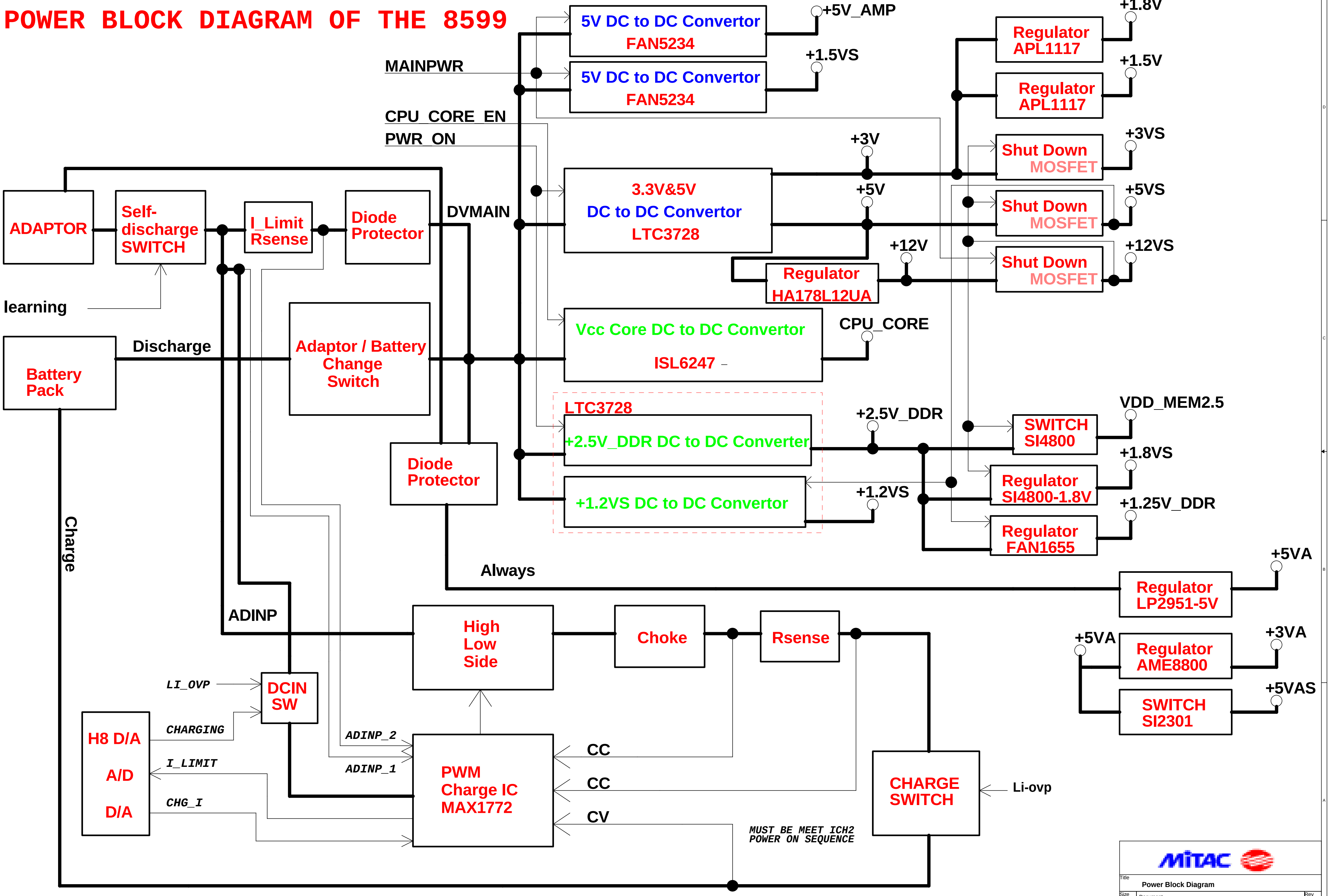
MiTAC

Title
SystemBlock DIAGRAM

Size | Document Number 411682900001 | Rev R06

Date: Monday, April 12, 2004 | Sheet 2 of 28

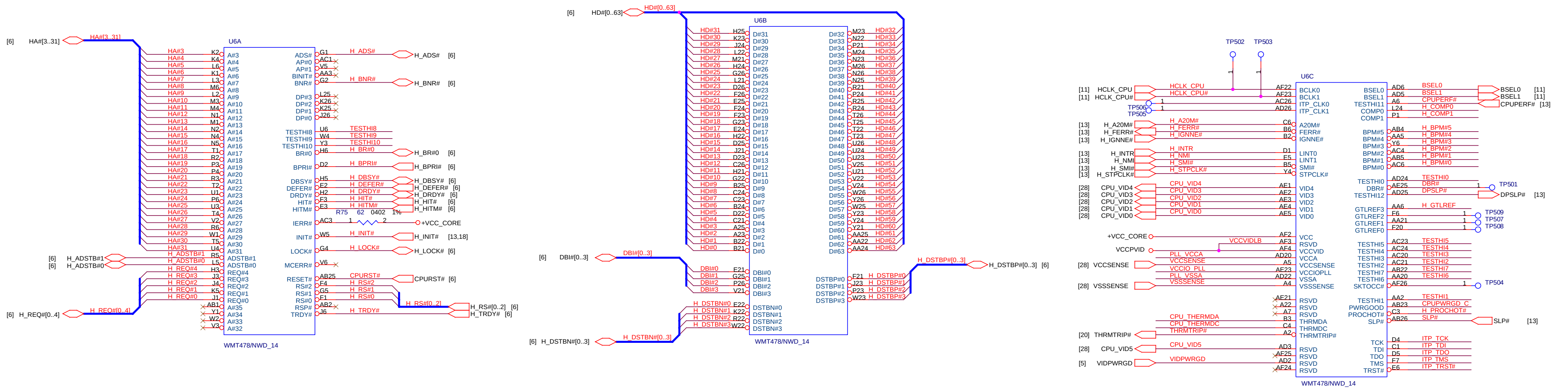
POWER BLOCK DIAGRAM OF THE 8599


5V DC to DC Convertor
FAN5234
+5V_AMP
MAINPWR
5V DC to DC Convertor
FAN5234
+1.5VS
CPU_CORE_EN
PWR_ON
Regulator
APL1117
+1.8V
Regulator
APL1117
+1.5V
Shut Down
MOSFET
+3VS
+3V
ADAPTOR
Self-
discharge
SWITCH
I_Limit
Rsense
Diode
Protector
DVMAIN
3.3V&5V
DC to DC Convertor
LTC3728
+5V
Shut Down
MOSFET
+5VS
+12V
Regulator
HA178L12UA
Shut Down
MOSFET
+12VS
learning
Vcc Core DC to DC Convertor
ISL6247
CPU_CORE
Battery
Pack
Discharge
Adaptor / Battery
Change
Switch
LTC3728
+2.5V_DDR DC to DC Converter
+2.5V_DDR
SWITCH
SI4800
VDD_MEM2.5
+1.2VS DC to DC Convertor
+1.2VS
Regulator
SI4800-1.8V
+1.8VS
Regulator
FAN1655
+1.25V_DDR
Diode
Protector
Charge
Always
Regulator
LP2951-5V
+5VA
ADINP
High
Low
Side
Choke
Rsense
+5VA
Regulator
AME8800
+3VA
SWITCH
SI2301
+5VAS
LI_OVP
DCIN
SW
CHARGING
H8 D/A
A/D
D/A
I_LIMIT
CHG_I
ADINP_2
ADINP_1
PWM
Charge IC
MAX1772
CC
CC
CV
CHARGE
SWITCH
Li-ovp
MUST BE MEET ICH2
POWER ON SEQUENCE

MiTAC

Title		
Power Block Diagram		
Size	Document Number 411682900001	Rev R06
Date: Monday, April 12, 2004	Sheet 3 of 28	

Prescott/Northwood (1/2)



U6A
HA#[3..31]
[6] HA#[3..31]
ADS#
BNR#
H_ADS# [6]
H_BNR# [6]
[6] H_ADSTB#1
[6] H_ADSTB#0
[6] H_REQ#[0..4]
H_BR#0 [6]
H_BPRI# [6]
H_DBSY# [6]
H_DEFER# [6]
H_DRDY# [6]
H_HIT# [6]
H_HITM# [6]
R75 62 0402 1%
+VCC_CORE
H_INIT# [13,18]
H_LOCK# [6]
CPURST# [6]
H_RS#[0..2] [6]
H_TRDY# [6]
WMT478/NWD_14
U6B
[6] HD#[0..63]
HD#[0..63]
[6] DBI#[0..3]
H_DSTBP#[0..3] [6]
[6] H_DSTBN#[0..3]
WMT478/NWD_14
U6C
TP502
TP503
[11] HCLK_CPU
[11] HCLK_CPU#
TP506
TP505
BSEL0 [11]
BSEL1 [11]
CPUPERF# [13]
[13] H_A20M#
[13] H_FERR#
[13] H_IGNNE#
[13] H_INTR
[13] H_NMI
[13] H_SMI#
[13] H_STPCLK#
[28] CPU_VID4
[28] CPU_VID3
[28] CPU_VID2
[28] CPU_VID1
[28] CPU_VID0
TP501
DPSLP# [13]
TP509
TP507
TP508
+VCC_CORE
VCCPVID
[28] VCCSENSE
[28] VSSSENSE
TP504
SLP# [13]
[20] THRMTRIP#
[28] CPU_VID5
[5] VIDPWRGD
WMT478/NWD_14

FSB SELECTION

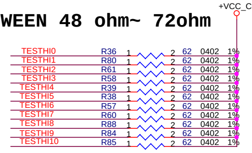
BSEL1	BSEL0	FUNCTION
0	0	100MHz
0	1	133MHz
1	0	200MHz
1	1	RESERVED

CPU Temperature Monitor

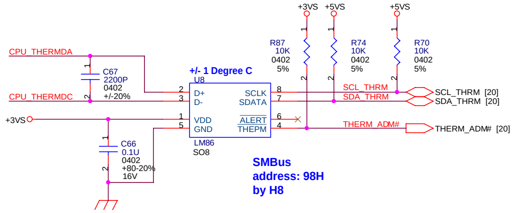
Placement : 3" (Maximum) From CPU

```
Mobile P4 533MHz impedance
is 50 between 40~60 ohm.
```

BETWEEN 48 ohm~ 72ohm

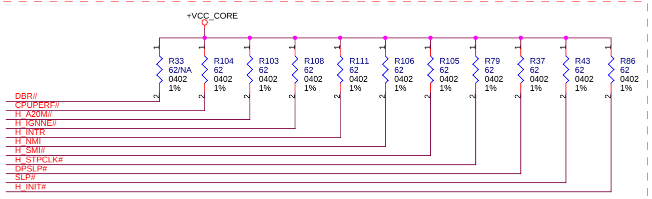


+VCC_CORE
TESTHI0 R36
TESTHI1 R80
TESTHI2 R61
TESTHI3 R58
TESTHI4 R39
TESTHI5 R38
TESTHI6 R57
TESTHI7 R60
TESTHI8 R88
TESTHI9 R84
TESTHI10 R85
62 0402 1%

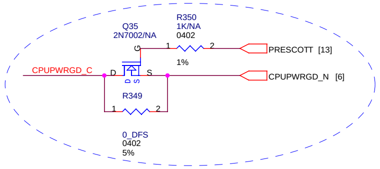


+3VS
+5VS
+5VS
R87 10K 0402 5%
R74 10K 0402 5%
R70 10K 0402 5%
CPU_THERMDA
CPU_THERMDC
C67 2200P 0402 +/-20%
+/- 1 Degree C
U8
D+
D-
SCLK
SDATA
VDD
GND
ALERT
THEPM
LM86
SO8
SCL_THRM
SDA_THRM
SCL_THRM [20]
SDA_THRM [20]
THERM_ADM#
THERM_ADM# [20]
+3VS
C66 0.1U 0402 +80-20% 16V

SMBus address: 98H by H8

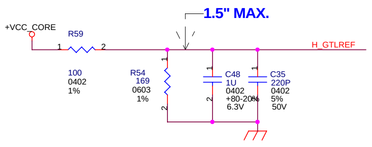


+VCC_CORE
R33 62/NA 0402 1%
R104 62 0402 1%
R103 62 0402 1%
R108 62 0402 1%
R111 62 0402 1%
R106 62 0402 1%
R105 62 0402 1%
R79 62 0402 1%
R37 62 0402 1%
R43 62 0402 1%
R86 62 0402 1%
DBR#
CPUPERF#
H_A20M#
H_IGNNE#
H_INTR
H_NMI
H_SMI#
H_STPCLK#
DPSLP#
SLP#
H_INIT#



Q35 2N7002/NA
R350 1K/NA 0402 1%
PRESCOTT [13]
CPUPWRGD_C
CPUPWRGD_N [6]
D
G
S
R349
0_DFS 0402 5%

GTL Reference CKT

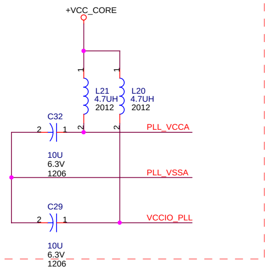


1.5" MAX.
+VCC_CORE
R59
H_GTLREF
100 0402 1%
R54 169 0603 1%
C48 1U 0402 +80-20% 6.3V
C35 220P 0402 5% 50V

One 220PF for each GTL REF Pin

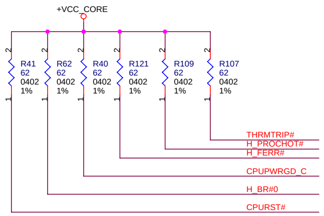
CLOSE TO CPU SOCKET

PLL SUPPLY FILTER



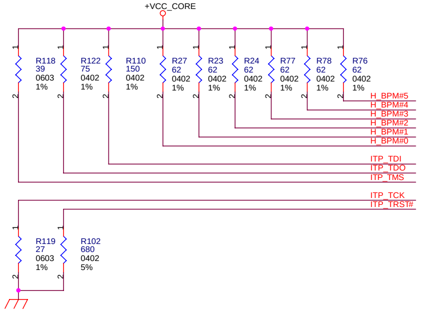
+VCC_CORE
L21 4.7UH 2012
L20 4.7UH 2012
C32
PLL_VCCA
10U 6.3V 1206
PLL_VSSA
C29
VCCIO_PLL
10U 6.3V 1206

CPU SIGNAL TERMINATION



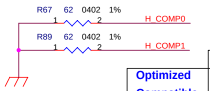
+VCC_CORE
R41 62 0402 1%
R62 62 0402 1%
R40 62 0402 1%
R121 62 0402 1%
R109 62 0402 1%
R107 62 0402 1%
THRMTRIP#
H_PROCHOT#
H_FERR#
CPUPWRGD_C
H_BR#0
CPURST#

PLACE CLOSE TO CPU SOCKET



+VCC_CORE
R118 39 0603 1%
R122 75 0402 1%
R110 150 0402 1%
R27 62 0402 1%
R23 62 0402 1%
R24 62 0402 1%
R77 62 0402 1%
R78 62 0402 1%
R76 62 0402 1%
H_BPM#5
H_BPM#4
H_BPM#3
H_BPM#2
H_BPM#1
H_BPM#0
ITP_TDI
ITP_TDO
ITP_TMS
ITP_TCK
ITP_TRST#
R119 27 0603 1%
R102 680 0402 5%

PRECISION FSB COMPENSATION RESISTORS



R67 62 0402 1%
H_COMP0
R89 62 0402 1%
H_COMP1

	COMP0/1
Optimized	49.9 1%
Compatible	61.9 1%

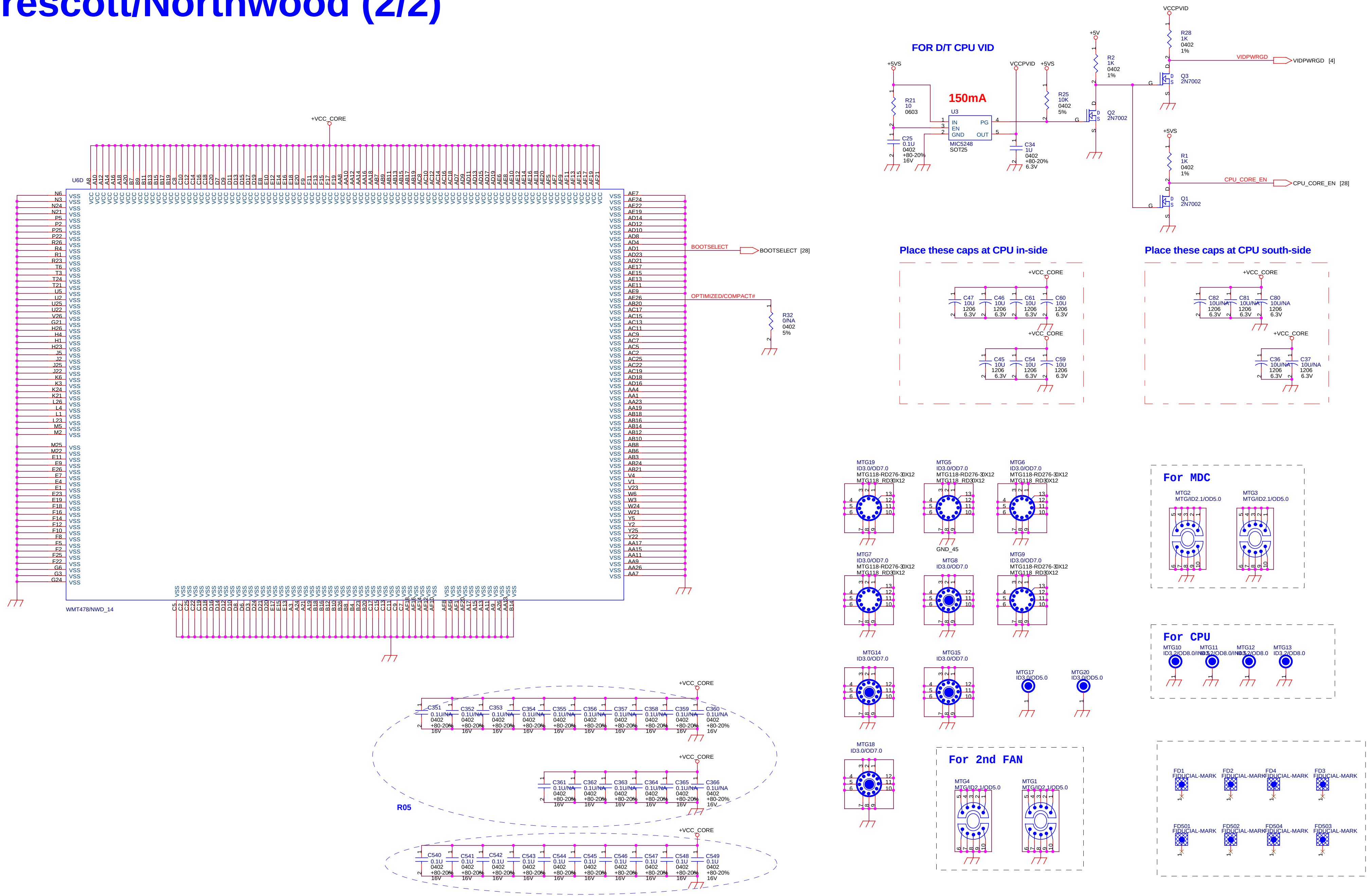
PLACE THESE INSIDE SOCKET CAVITY

Title
Prescott/Northwood (1/2)

Size | Document Number 411682900001 | Rev R06

Date: Monday, April 12, 2004 | Sheet 4 of 28

Prescott/Northwood (2/2)


FOR D/T CPU VID
150mA
+5VS
VCCPVID
+5V
R21 10 0603
C25 0.1U 0402 +80-20% 16V
U3 MIC5248 SOT25
IN EN GND PG OUT
C34 1U 0402 +80-20% 6.3V
R25 10K 0402 5%
Q2 2N7002
R2 1K 0402 1%
R28 1K 0402 1%
Q3 2N7002
VIDPWRGD
VIDPWRGD [4]
R1 1K 0402 1%
Q1 2N7002
CPU_CORE_EN
CPU_CORE_EN [28]
+VCC_CORE
U6D
WMT478/NWD_14
BOOTSELECT
BOOTSELECT [28]
OPTIMIZED/COMPACT#
R32 0/NA 0402 5%
Place these caps at CPU in-side
C47 10U 1206 6.3V
C46 10U 1206 6.3V
C61 10U 1206 6.3V
C60 10U 1206 6.3V
C45 10U 1206 6.3V
C54 10U 1206 6.3V
C59 10U 1206 6.3V
Place these caps at CPU south-side
C82 10U/NA 1206 6.3V
C81 10U/NA 1206 6.3V
C80 10U/NA 1206 6.3V
C36 10U/NA 1206 6.3V
C37 10U/NA 1206 6.3V
MTG19 ID3.0/OD7.0 MTG118-RD276-3X12
MTG5 ID3.0/OD7.0 MTG118-RD276-3X12
MTG6 ID3.0/OD7.0 MTG118-RD276-3X12
GND_45
MTG7 ID3.0/OD7.0 MTG118-RD276-3X12
MTG8 ID3.0/OD7.0
MTG9 ID3.0/OD7.0 MTG118-RD276-3X12
MTG14 ID3.0/OD7.0
MTG15 ID3.0/OD7.0
MTG17 ID3.0/OD5.0
MTG20 ID3.0/OD5.0
MTG18 ID3.0/OD7.0
For MDC
MTG2 MTG/ID2.1/OD5.0
MTG3 MTG/ID2.1/OD5.0
For CPU
MTG10 ID3.2/OD8.0/NA
MTG11 ID3.2/OD8.0/NA
MTG12 ID3.2/OD8.0
MTG13 ID3.2/OD8.0
For 2nd FAN
MTG4 MTG/ID2.1/OD5.0
MTG1 MTG/ID2.1/OD5.0
FD1 FIDUCIAL-MARK
FD2 FIDUCIAL-MARK
FD4 FIDUCIAL-MARK
FD3 FIDUCIAL-MARK
FD501 FIDUCIAL-MARK
FD502 FIDUCIAL-MARK
FD504 FIDUCIAL-MARK
FD503 FIDUCIAL-MARK
C351 0.1U/NA 0402 +80-20% 16V
C352 0.1U/NA 0402 +80-20% 16V
C353 0.1U/NA 0402 +80-20% 16V
C354 0.1U/NA 0402 +80-20% 16V
C355 0.1U/NA 0402 +80-20% 16V
C356 0.1U/NA 0402 +80-20% 16V
C357 0.1U/NA 0402 +80-20% 16V
C358 0.1U/NA 0402 +80-20% 16V
C359 0.1U/NA 0402 +80-20% 16V
C360 0.1U/NA 0402 +80-20% 16V
C361 0.1U/NA 0402 +80-20% 16V
C362 0.1U/NA 0402 +80-20% 16V
C363 0.1U/NA 0402 +80-20% 16V
C364 0.1U/NA 0402 +80-20% 16V
C365 0.1U/NA 0402 +80-20% 16V
C366 0.1U/NA 0402 +80-20% 16V
R05
C540 0.1U 0402 +80-20% 16V
C541 0.1U 0402 +80-20% 16V
C542 0.1U 0402 +80-20% 16V
C543 0.1U 0402 +80-20% 16V
C544 0.1U 0402 +80-20% 16V
C545 0.1U 0402 +80-20% 16V
C546 0.1U 0402 +80-20% 16V
C547 0.1U 0402 +80-20% 16V
C548 0.1U 0402 +80-20% 16V
C549 0.1U 0402 +80-20% 16V
R06

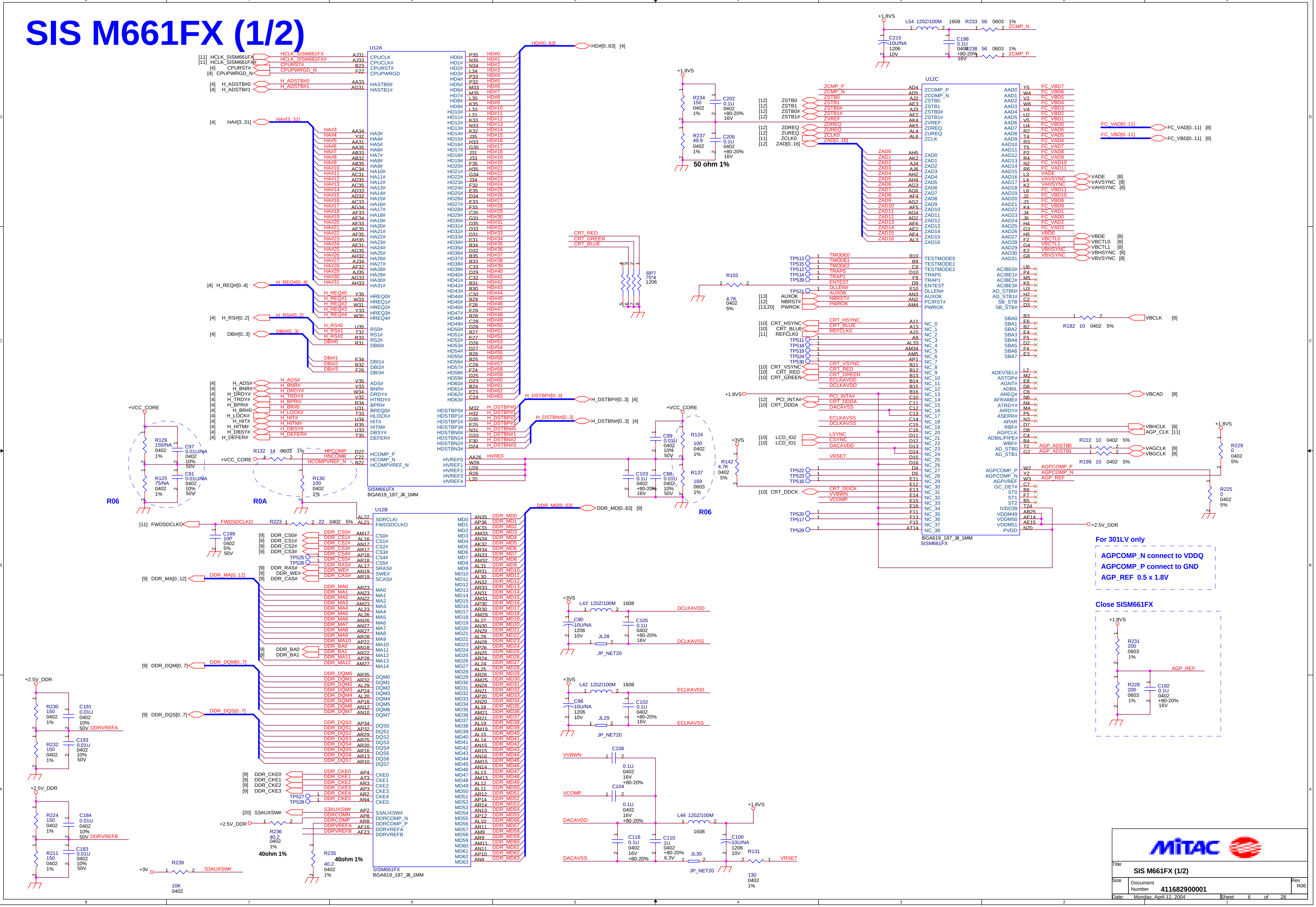
MiTAC

Title
Prescott/Northwood (2/2)

Size	Document Number	Rev
	411682900001	R06

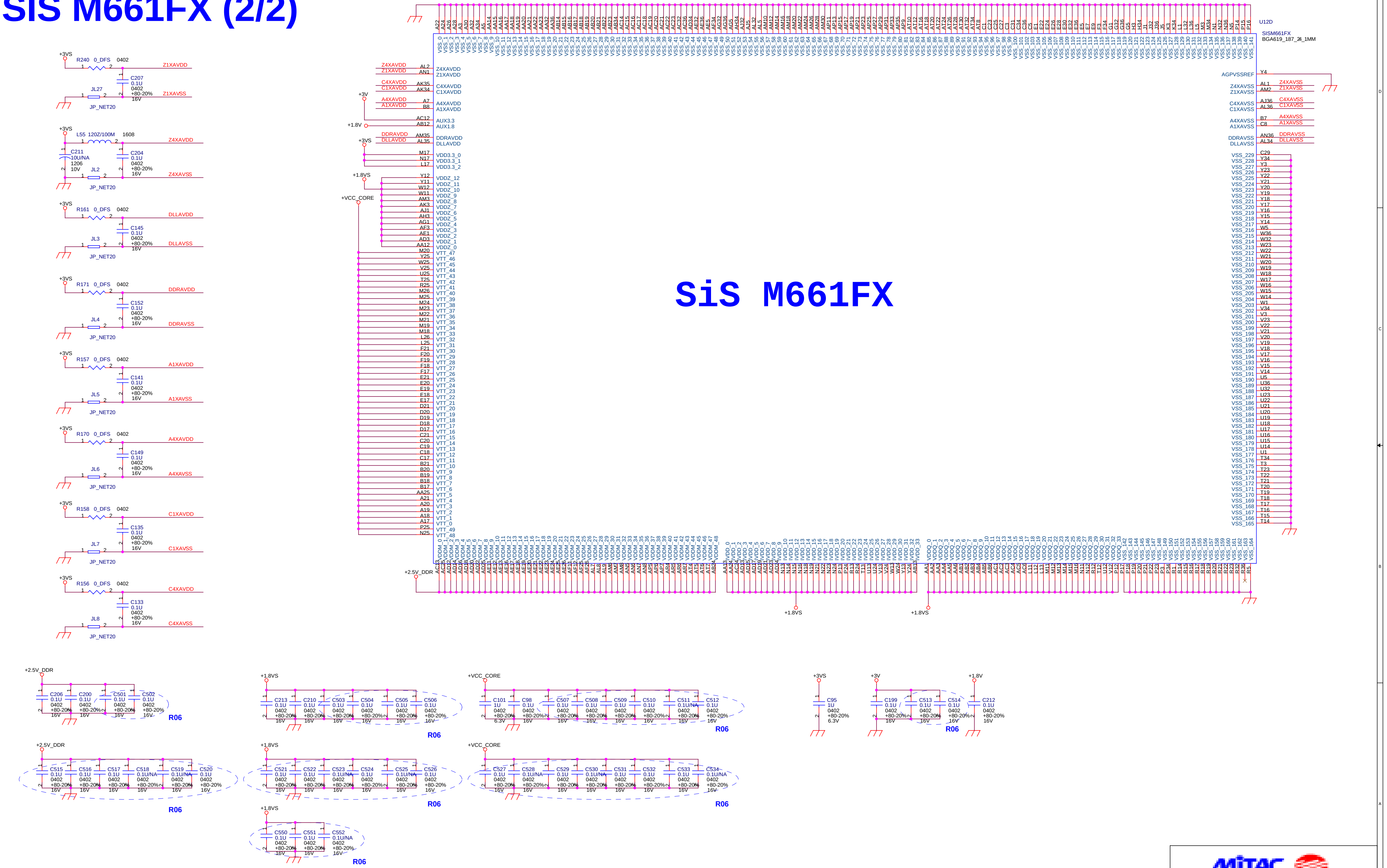
Date: Monday, April 12, 2004 Sheet 5 of 28

SIS M661FX (1/2)


U12A
U12B
U12C
SISM661FX
BGA619_187_24_1MM
HCLK_SISM661FX
HCLK_SISM661FX#
CPURST#
CPUPWRGD_N
H_ADSTB#0
H_ADSTB#1
HA#[3..31]
HD#[0..63]
H_REQ#[0..4]
H_RS#[0..2]
DBI#[0..3]
H_ADS#
H_BNR#
H_DRDY#
H_TRDY#
H_BPRI#
H_BR#0
H_LOCK#
H_HIT#
H_HITM#
H_DBSY#
H_DEFER#
H_DSTBP#[0..3]
H_DSTBN#[0..3]
HCOMP_P
HCOMP_N
HCOMPVREF_N
HVREF
+VCC_CORE
R129 150/NA 0402 1%
C97 0.01U/NA 0402 10% 50V
R125 75/NA 0402 1%
C91 0.01U/NA 0402 10% 50V
R132 14 0603 1%
R130 100 0402 1%
C99 0.01U 0402 10% 50V
R124 100 0402 1%
C103 0.1U 0402 +80-20% 16V
C88 0.01U 0402 10% 50V
R137 169 0603 1%
R142 4.7K 0402 5%
R06
R0A
FWDSDCLKO
R223 22 0402 5%
C189 10P 0402 5% 50V
DDR_CS0# DDR_CS1# DDR_CS2# DDR_CS3#
DDR_RAS# DDR_WE# DDR_CAS#
DDR_MA[0..12]
DDR_BA0 DDR_BA1
DDR_DQM[0..7]
DDR_DQS[0..7]
DDR_CKE0 DDR_CKE1 DDR_CKE2 DDR_CKE3
S3AUXSW#
DDRCOMP_N
DDRCOMP_P
DDRVREFA
DDRVREFB
DDR_MD[0..63]
R236 40.2 0402 1%
40ohm 1%
R235 40.2 0402 1%
40ohm 1%
R239 10K 0402
+2.5V_DDR
R230 150 0402 1%
C191 0.01U 0402 10% 50V
R232 150 0402 1%
C193 0.01U 0402 10% 50V
R224 150 0402 1%
C184 0.01U 0402 10% 50V
R211 150 0402 1%
C183 0.01U 0402 10% 50V
+1.8VS
L54 120Z/100M 1608
R233 56 0603 1%
ZCMP_N
C215 10U/NA 1206 10V
C198 0.1U 0402 +80-20% 16V
R238 56 0603 1%
ZCMP_P
R234 150 0402 1%
C202 0.1U 0402 +80-20% 16V
R237 49.9 0402 1%
C205 0.1U 0402 +80-20% 16V
50 ohm 1%
ZSTB0 ZSTB1 ZSTB0# ZSTB1#
ZDREQ ZUREQ ZCLK0
ZAD[0..16]
CRT_RED CRT_GREEN CRT_BLUE
RP7 75*4 1206
R155 4.7K 0402 5%
AUXOK NBRST# PWROK
CRT_HSYNC CRT_BLUE REFCLK0
CRT_VSYNC CRT_RED CRT_GREEN
PCI_INTA#
CRT_DDDA
LCD_ID2 LCD_ID1
CRT_DDCK
FC_VAD[0..11]
FC_VBD[0..11]
VADE VAVSYNC VAHSYNC
VBDE VBCTL0 VBCTL1 VBHSYNC VBVSYNC
VBCLK
R182 10 0402 5%
VBCAD
VBHCLK
AGP_CLK
R222 10 0402 5%
R199 10 0402 5%
VAGCLK VBGCLK
R229 0 0402 5%
R225 0 0402 5%
AGPCOMP_P AGPCOMP_N AGP_REF
+2.5V_DDR
For 301LV only
AGPCOMP_N connect to VDDQ
AGPCOMP_P connect to GND
AGP_REF 0.5 x 1.8V
Close SISM661FX
R231 200 0603 1%
R228 200 0603 1%
C192 0.1U 0402 +80-20% 16V
+3VS
L43 120Z/100M 1608
C90 10U/NA 1206 10V
C105 0.1U 0402 +80-20% 16V
JL28 JP_NET20
DCLKAVDD DCLKAVSS
L42 120Z/100M 1608
C96 10U/NA 1206 10V
C102 0.1U 0402 +80-20% 16V
JL29 JP_NET20
ECLKAVDD ECLKAVSS
VVBWN
C106 0.1U 0402 16V +80-20%
VCOMP
C104 0.1U 0402 16V +80-20%
DACAVDD
L44 120Z/100M 1608
C116 0.1U 0402 16V +80-20%
C110 1U 0402 +80-20% 6.3V
C100 10U/NA 1206 10V
DACAVSS
JL30 JP_NET20
R131 130 0402 1%
VRSET

Title	SIS M661FX (1/2)
Size	Document Number 411682900001
Rev	R06
Date:	Monday, April 12, 2004
Sheet	6 of 28

SIS M661FX (2/2)


SiS M661FX
U12D
SISM661FX
BGA619_187_24_1MM
+3VS
R240 0_DFS 0402
Z1XAVDD
C207 0.1U 0402 +80-20% 16V
JL27
JP_NET20
Z1XAVSS
L55 120Z/100M 1608
Z4XAVDD
C211 10U/NA 1206 10V
C204 0.1U 0402 +80-20% 16V
JL2
Z4XAVSS
R161 0_DFS 0402
DLLAVDD
C145 0.1U 0402 +80-20% 16V
JL3
DLLAVSS
R171 0_DFS 0402
DDRAVDD
C152 0.1U 0402 +80-20% 16V
JL4
DDRAVSS
R157 0_DFS 0402
A1XAVDD
C141 0.1U 0402 +80-20% 16V
JL5
A1XAVSS
R170 0_DFS 0402
A4XAVDD
C149 0.1U 0402 +80-20% 16V
JL6
A4XAVSS
R158 0_DFS 0402
C1XAVDD
C135 0.1U 0402 +80-20% 16V
JL7
C1XAVSS
R156 0_DFS 0402
C4XAVDD
C133 0.1U 0402 +80-20% 16V
JL8
C4XAVSS
+3V
+1.8V
AUX3.3
AUX1.8
VDD3.3_0
VDD3.3_1
VDD3.3_2
+1.8VS
+VCC_CORE
VDDZ_0 … VDDZ_12
VTT_0 … VTT_49
AGPVSSREF
VSS_0 … VSS_229
+2.5V_DDR
VDDM_0 … VDDM_48
IVDD_0 … IVDD_33
VDDQ_0 … VDDQ_33
C206 0.1U 0402 +80-20% 16V
C200 0.1U
C501 0.1U
C502 0.1U
R06
C213 0.1U
C210 0.1U
C503 0.1U
C504 0.1U
C505 0.1U
C506 0.1U
C101 1U 0402 +80-20% 6.3V
C98 0.1U
C507 0.1U
C508 0.1U
C509 0.1U
C510 0.1U
C511 0.1U/NA
C512 0.1U
C95 1U 0402 +80-20% 6.3V
C199 0.1U
C513 0.1U
C514 0.1U
C212 0.1U
C515 0.1U
C516 0.1U
C517 0.1U
C518 0.1U/NA
C519 0.1U/NA
C520 0.1U
C521 0.1U
C522 0.1U
C523 0.1U/NA
C524 0.1U
C525 0.1U/NA
C526 0.1U
C527 0.1U
C528 0.1U/NA
C529 0.1U
C530 0.1U/NA
C531 0.1U
C532 0.1U
C533 0.1U
C534 0.1U/NA
C550 0.1U
C551 0.1U
C552 0.1U/NA
8 7 6 5 4 3 2 1
D C B A

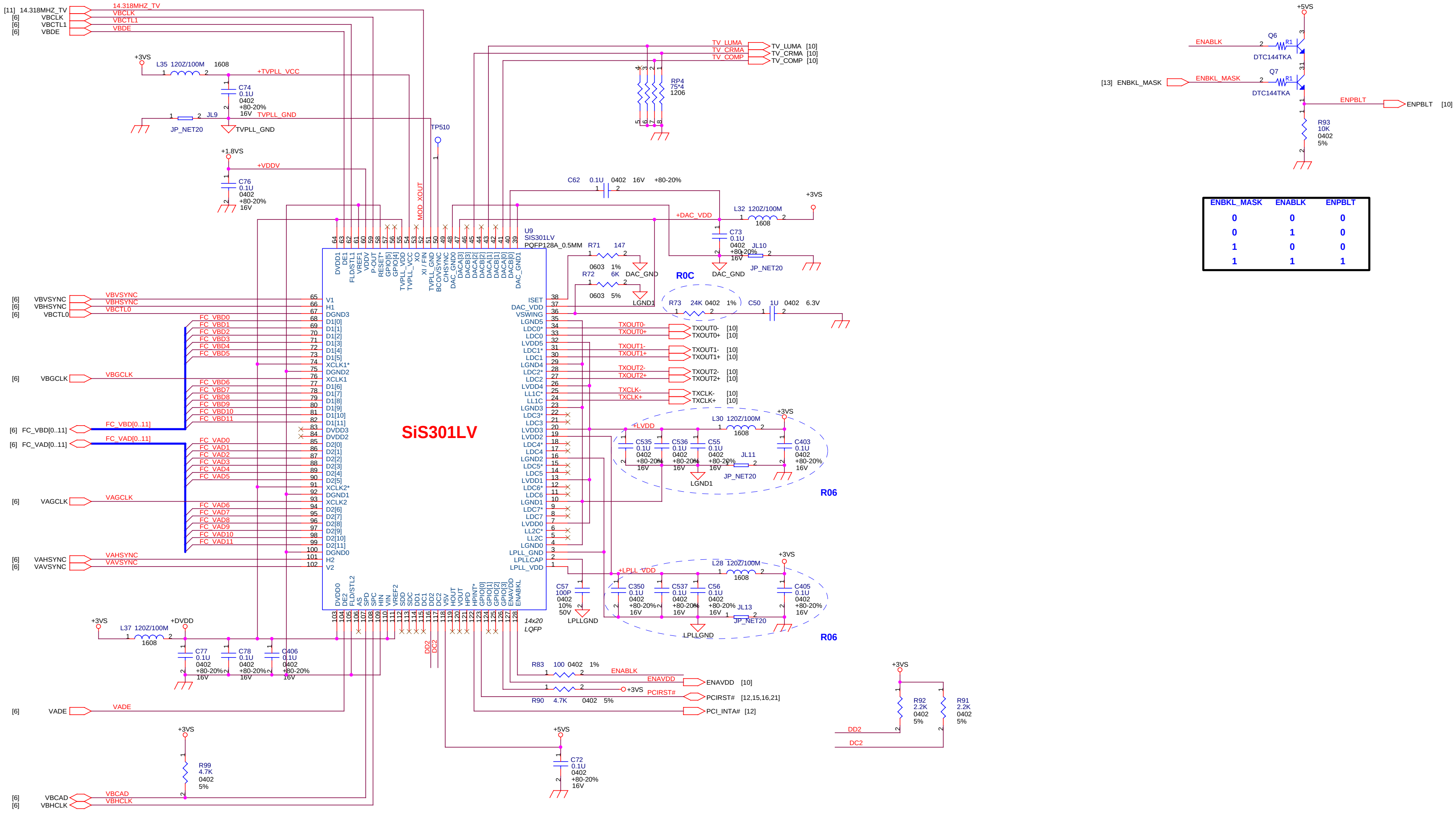
MiTAC

Title
SIS M661FX (2/2)

Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 7 of 28

TV/LVDS ENCODER (SIS301LV)


SiS301LV
U9
SIS301LV
PQFP128A_0.5MM
14x20
LQFP
[11] 14.318MHZ_TV
[6] VBCLK
[6] VBCTL1
[6] VBDE
14.318MHZ_TV
VBCLK
VBCTL1
VBDE
+3VS
L35 120Z/100M 1608
+TVPLL_VCC
C74 0.1U 0402 +80-20% 16V
JL9
JP_NET20
TVPLL_GND
TP510
+1.8VS
+VDDV
C76 0.1U 0402 +80-20% 16V
MOD_XOUT
TV_LUMA
TV_CRMA
TV_COMP
TV_LUMA [10]
TV_CRMA [10]
TV_COMP [10]
RP4 75*4 1206
C62 0.1U 0402 16V +80-20%
+3VS
L32 120Z/100M 1608
+DAC_VDD
C73 0.1U 0402 +80-20% 16V
JL10
JP_NET20
DAC_GND
R71 147 0603 1%
R72 6K 0603 5%
R0C
R73 24K 0402 1%
C50 1U 0402 6.3V
LGND1
[6] VBVSYNC
[6] VBHSYNC
[6] VBCTL0
VBVSYNC
VBHSYNC
VBCTL0
FC_VBD0
FC_VBD1
FC_VBD2
FC_VBD3
FC_VBD4
FC_VBD5
[6] VBGCLK
VBGCLK
FC_VBD6
FC_VBD7
FC_VBD8
FC_VBD9
FC_VBD10
FC_VBD11
[6] FC_VBD[0..11]
[6] FC_VAD[0..11]
FC_VBD[0..11]
FC_VAD[0..11]
FC_VAD0
FC_VAD1
FC_VAD2
FC_VAD3
FC_VAD4
FC_VAD5
[6] VAGCLK
VAGCLK
FC_VAD6
FC_VAD7
FC_VAD8
FC_VAD9
FC_VAD10
FC_VAD11
[6] VAHSYNC
[6] VAVSYNC
VAHSYNC
VAVSYNC
V1
H1
DGND3
D1[0]
D1[1]
D1[2]
D1[3]
D1[4]
D1[5]
XCLK1*
DGND2
XCLK1
D1[6]
D1[7]
D1[8]
D1[9]
D1[10]
D1[11]
DVDD3
DVDD2
D2[0]
D2[1]
D2[2]
D2[3]
D2[4]
D2[5]
XCLK2*
DGND1
XCLK2
D2[6]
D2[7]
D2[8]
D2[9]
D2[10]
D2[11]
DGND0
H2
V2
DVDD1
DE1
FLD/STL1
VREF1
VDDV
P-OUT
RESET*
GPIO[5]
GPIO[4]
TVPLL_VDD
TVPLL_VCC
XI / FIN
XO
TVPLL_GND
BCO/VSYNC
C/HSYNC
DAC_GND0
DACB[3]
DACA[3]
DACB[2]
DACA[2]
DACB[1]
DACA[1]
DACB[0]
DACA[0]
DAC_GND1
ISET
DAC_VDD
VSWING
LGND5
LDC0*
LDC0
LVDD5
LDC1*
LDC1
LGND4
LDC2*
LDC2
LVDD4
LL1C*
LL1C
LGND3
LDC3*
LDC3
LVDD3
LVDD2
LDC4*
LDC4
LGND2
LDC5*
LDC5
LVDD1
LDC6*
LDC6
LGND1
LDC7*
LDC7
LVDD0
LL2C*
LL2C
LGND0
LPLL_GND
LPLLCAP
LPLL_VDD
DVDD0
DE2
FLD/STL2
AS
SPD
SPC
HIN
VIN
VREF2
SDD
SDC
VD1
DC1
DD2
DC2
V5V
VOUT
HPD
PINT*
GPIO[0]
GPIO[1]
GPIO[2]
GPIO[3]
ENAVDD
ENABKL
TXOUT0-
TXOUT0+
TXOUT1-
TXOUT1+
TXOUT2-
TXOUT2+
TXCLK-
TXCLK+
TXOUT0- [10]
TXOUT0+ [10]
TXOUT1- [10]
TXOUT1+ [10]
TXOUT2- [10]
TXOUT2+ [10]
TXCLK- [10]
TXCLK+ [10]
+3VS
L30 120Z/100M 1608
+LVDD
C535 0.1U 0402 +80-20% 16V
C536 0.1U 0402 +80-20% 16V
C55 0.1U 0402 +80-20% 16V
C403 0.1U 0402 +80-20% 16V
JL11
JP_NET20
LGND1
R06
+3VS
L28 120Z/100M 1608
+LPLL_VDD
C57 100P 0402 10% 50V
LPLLGND
C350 0.1U 0402 +80-20% 16V
C537 0.1U 0402 +80-20% 16V
C56 0.1U 0402 +80-20% 16V
C405 0.1U 0402 +80-20% 16V
JL13
JP_NET20
LPLLGND
R06
+3VS
L37 120Z/100M 1608
+DVDD
C77 0.1U 0402 +80-20% 16V
C78 0.1U 0402 +80-20% 16V
C406 0.1U 0402 +80-20% 16V
[6] VADE
VADE
+3VS
R99 4.7K 0402 5%
[6] VBCAD
[6] VBHCLK
VBCAD
VBHCLK
DD2
DC2
+5VS
C72 0.1U 0402 +80-20% 16V
R83 100 0402 1%
ENABLK
ENAVDD
ENAVDD [10]
+3VS
PCIRST#
PCIRST# [12,15,16,21]
R90 4.7K 0402 5%
PCI_INTA# [12]
+3VS
R92 2.2K 0402 5%
R91 2.2K 0402 5%
DD2
DC2
+5VS
ENABLK
Q6
R1
DTC144TKA
[13] ENBKL_MASK
ENBKL_MASK
Q7
R1
DTC144TKA
ENPBLT
ENPBLT [10]
R93 10K 0402 5%

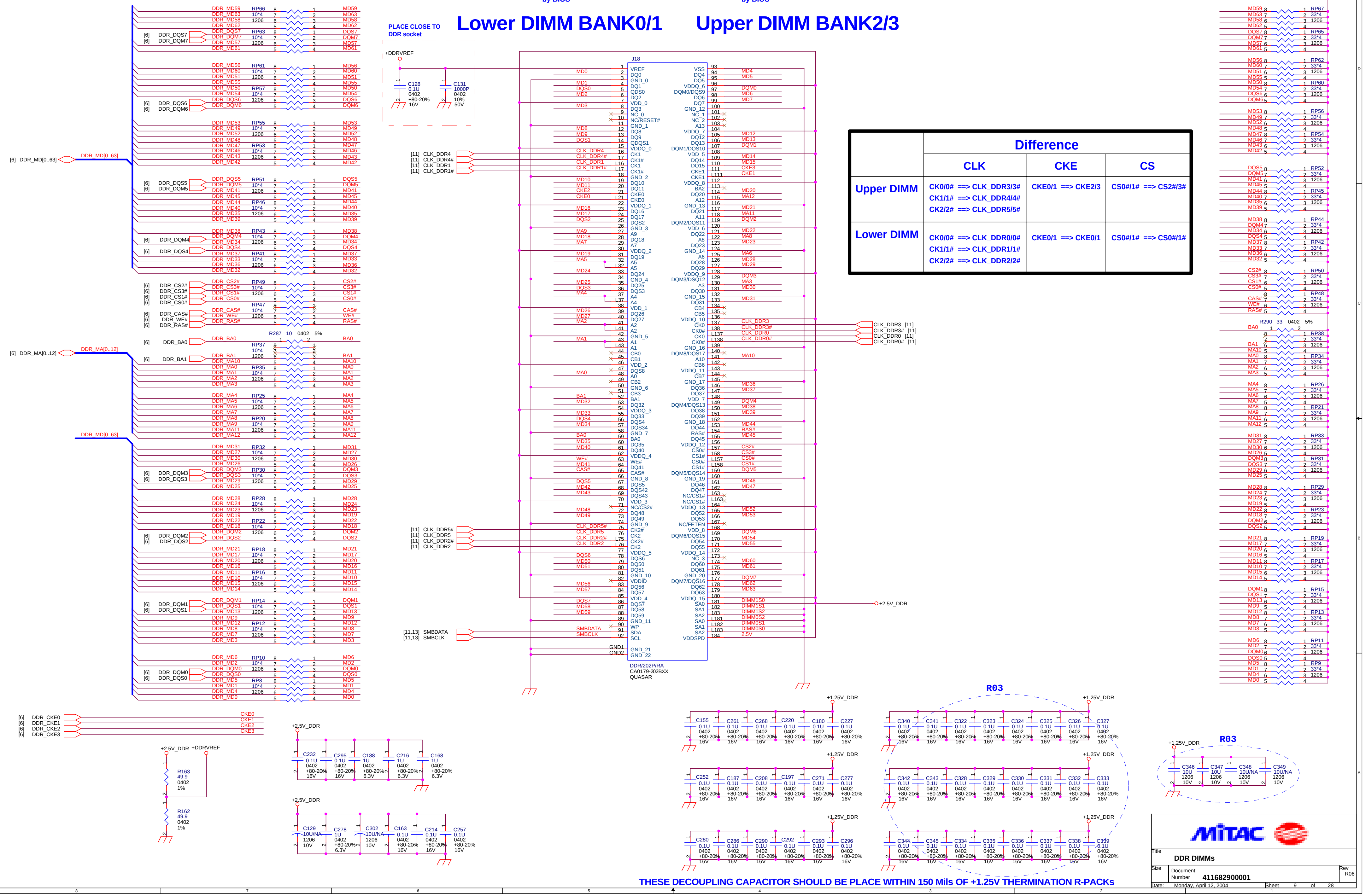
ENBKL_MASK	ENABLK	ENPBLT
0	0	0
0	1	0
1	0	0
1	1	1

Title
TV/LVDS ENCODER (SIS301LV)

Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 8 of 28

DDR DIMMs


SMBus
address: A0h
by BIOS
SMBus
address: A2h
by BIOS
Lower DIMM BANK0/1
Upper DIMM BANK2/3
PLACE CLOSE TO
DDR socket
+DDRVREF
C128 0.1U 0402 +80-20% 16V
C131 1000P 0402 10% 50V
J18
DDR/202P/RA
CA0179-202BXX
QUASAR
[6] DDR_MD[0..63]
[6] DDR_MA[0..12]
[11] CLK_DDR4
[11] CLK_DDR4#
[11] CLK_DDR1
[11] CLK_DDR1#
[11] CLK_DDR5#
[11] CLK_DDR5
[11] CLK_DDR2#
[11] CLK_DDR2
CLK_DDR3 [11]
CLK_DDR3# [11]
CLK_DDR0 [11]
CLK_DDR0# [11]
[11,13] SMBDATA
[11,13] SMBCLK
+2.5V_DDR
+1.25V_DDR
R287 10 0402 5%
R290 33 0402 5%
[6] DDR_CKE0
[6] DDR_CKE1
[6] DDR_CKE2
[6] DDR_CKE3
R163 49.9 0402 1%
R162 49.9 0402 1%
R03
C346 10U 1206 10V
C347 10U 1206 10V
C348 10U/NA 1206 10V
C349 10U/NA 1206 10V

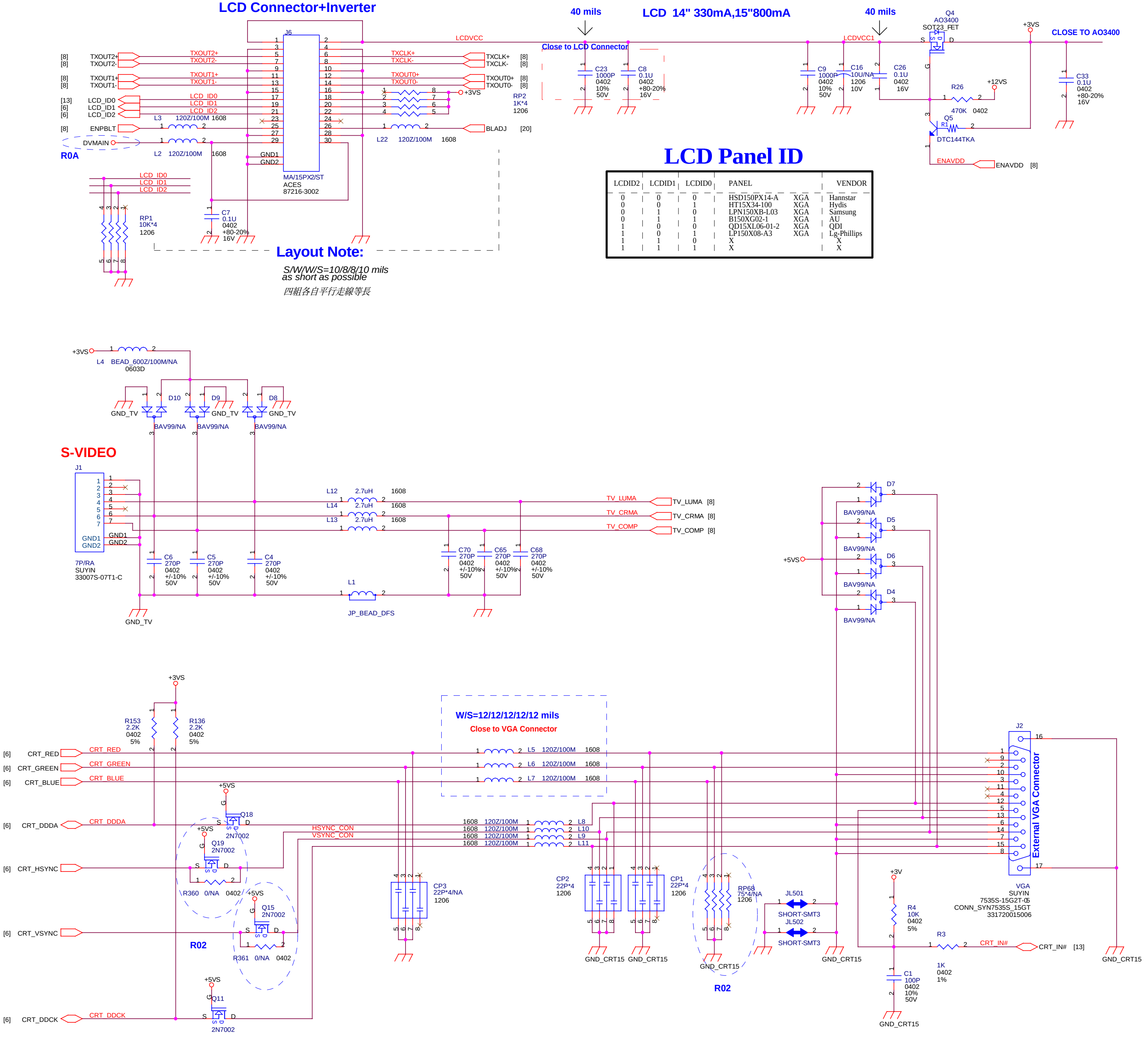
<table>
<tr><th rowspan="2"></th><th colspan="3">Difference</th></tr>
<tr><th>CLK</th><th>CKE</th><th>CS</th></tr>
<tr><td>Upper DIMM</td><td>CK0/0# ==> CLK_DDR3/3#
CK1/1# ==> CLK_DDR4/4#
CK2/2# ==> CLK_DDR5/5#</td><td>CKE0/1 ==> CKE2/3</td><td>CS0#/1# ==> CS2#/3#</td></tr>
<tr><td>Lower DIMM</td><td>CK0/0# ==> CLK_DDR0/0#
CK1/1# ==> CLK_DDR1/1#
CK2/2# ==> CLK_DDR2/2#</td><td>CKE0/1 ==> CKE0/1</td><td>CS0#/1# ==> CS0#/1#</td></tr>
</table>

THESE DECOUPLING CAPACITOR SHOULD BE PLACE WITHIN 150 Mils OF +1.25V THERMINATION R-PACKs

MiTAC

Title	**DDR DIMMs**	
Size	Document Number **411682900001**	Rev R06
Date: Monday, April 12, 2004	Sheet 9 of 28	

LCD / VGA Interface


LCD Connector+Inverter
J6
MA/15PX2/ST
ACES
87216-3002
TXOUT2+
TXOUT2-
TXOUT1+
TXOUT1-
LCD_ID0
LCD_ID1
LCD_ID2
ENPBLT
DVMAIN
R0A
TXCLK+
TXCLK-
TXOUT0+
TXOUT0-
BLADJ
LCDVCC
+3VS
RP2
1K*4
1206
L3 120Z/100M 1608
L2 120Z/100M 1608
L22 120Z/100M 1608
GND1
GND2
RP1
10K*4
1206
C7
0.1U
0402
+80-20%
16V
40 mils
Close to LCD Connector
C23
1000P
0402
10%
50V
C8
0.1U
0402
+80-20%
16V
LCD 14" 330mA,15"800mA
LCDVCC1
C9
1000P
0402
10%
50V
C16
10U/NA
1206
10V
C26
0.1U
0402
16V
Q4
AO3400
SOT23_FET
+3VS
CLOSE TO AO3400
C33
0.1U
0402
+80-20%
16V
R26
470K 0402
+12VS
Q5
R1
DTC144TKA
ENAVDD
Layout Note:
S/W/W/S=10/8/8/10 mils
as short as possible
四組各自平行走線等長
+3VS
L4 BEAD_600Z/100M/NA
0603D
GND_TV
D10
D9
D8
BAV99/NA
S-VIDEO
J1
7P/RA
SUYIN
33007S-07T1-C
L12 2.7uH 1608
L14 2.7uH 1608
L13 2.7uH 1608
TV_LUMA
TV_CRMA
TV_COMP
C6 270P 0402 +/-10% 50V
C5 270P 0402 +/-10% 50V
C4 270P 0402 +/-10% 50V
C70 270P 0402 +/-10% 50V
C65 270P 0402 +/-10% 50V
C68 270P 0402 +/-10% 50V
L1
JP_BEAD_DFS
D7
D5
D6
D4
BAV99/NA
+5VS
+3VS
R153 2.2K 0402 5%
R136 2.2K 0402 5%
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_DDDA
CRT_HSYNC
CRT_VSYNC
CRT_DDCK
Q18 2N7002
Q19 2N7002
Q15 2N7002
Q11 2N7002
R360 0/NA 0402
R361 0/NA 0402
R02
HSYNC_CON
VSYNC_CON
W/S=12/12/12/12 mils
Close to VGA Connector
L5 120Z/100M 1608
L6 120Z/100M 1608
L7 120Z/100M 1608
L8 120Z/100M 1608
L10 120Z/100M 1608
L9 120Z/100M 1608
L11 120Z/100M 1608
CP3 22P*4/NA 1206
CP2 22P*4 1206
CP1 22P*4 1206
RP68 75*4/NA 1206
GND_CRT15
JL501 SHORT-SMT3
JL502 SHORT-SMT3
+3V
R4 10K 0402 5%
R3 1K 0402 1%
C1 100P 0402 10% 50V
CRT_IN#
J2
External VGA Connector
VGA
SUYIN
7535S-15G2T-05
CONN_SYN7535S_15GT
331720015006

LCD Panel ID

LCDID2	LCDID1	LCDID0	PANEL		VENDOR
0	0	0	HSD150PX14-A	XGA	Hannstar
0	0	1	HT15X34-100	XGA	Hydis
0	1	0	LPN150XB-L03	XGA	Samsung
0	1	1	B150XG02-1	XGA	AU
1	0	0	QD15XL06-01-2	XGA	QDI
1	0	1	LP150X08-A3	XGA	Lg-Phillips
1	1	0	X		X
1	1	1	X		X

MiTAC

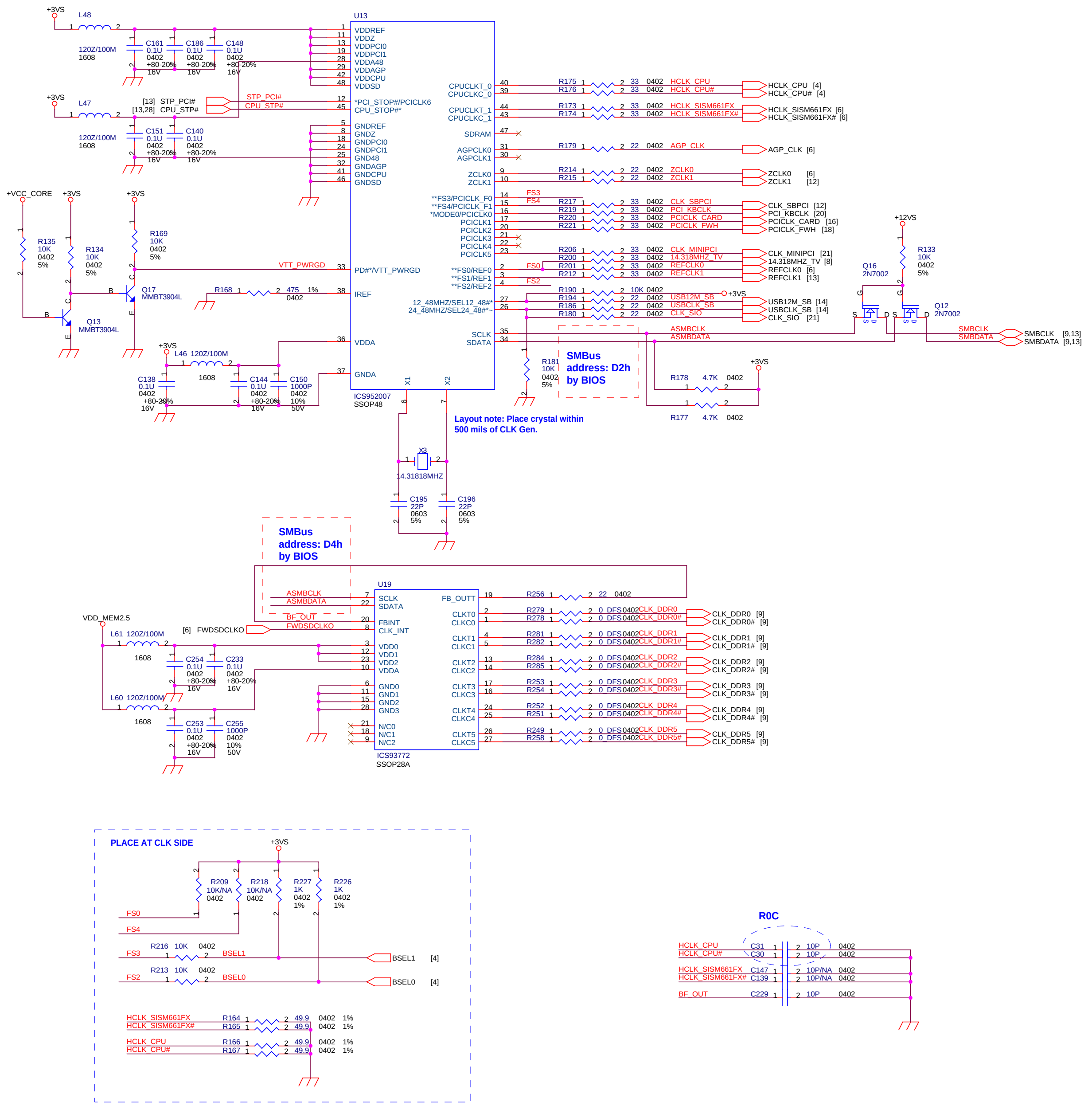
Title
LCD / VGA Interface

Size
Document Number **411682900001**
Rev R06

Date: Monday, April 12, 2004
Sheet 10 of 28

Clock Generator/Buffer

*** INTERNAL PULL UP RESISTOR**
**** INTERNAL PULL DOWN RESISTOR**
~ THIS OUTPUT HAS 1.5X DRIVE STRENGTH



+3VS
L48
120Z/100M
1608
C161 0.1U 0402 +80-20% 16V
C186 0.1U 0402 +80-20% 16V
C148 0.1U 0402 +80-20% 16V
L47
C151 0.1U 0402 +80-20% 16V
C140 0.1U 0402 +80-20% 16V
[13] STP_PCI#
[13,28] CPU_STP#
STP_PCI#
CPU_STP#
U13
VDDREF
VDDZ
VDDPCI0
VDDPCI1
VDDA48
VDDAGP
VDDCPU
VDDSD
*PCI_STOP#/PCICLK6
CPU_STOP#*
GNDREF
GNDZ
GNDPCI0
GNDPCI1
GND48
GNDAGP
GNDCPU
GNDSD
PD#*/VTT_PWRGD
IREF
VDDA
GNDA
X1
X2
ICS952007
SSOP48
CPUCLKT_0
CPUCLKC_0
CPUCLKT_1
CPUCLKC_1
SDRAM
AGPCLK0
AGPCLK1
ZCLK0
ZCLK1
**FS3/PCICLK_F0
**FS4/PCICLK_F1
*MODE0/PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5
**FS0/REF0
**FS1/REF1
**FS2/REF2
12_48MHZ/SEL12_48#*
24_48MHZ/SEL24_48#*~
SCLK
SDATA
+VCC_CORE
R135 10K 0402 5%
R134 10K 0402 5%
R169 10K 0402 5%
VTT_PWRGD
Q17 MMBT3904L
Q13 MMBT3904L
R168 475 1% 0402
L46 120Z/100M
C138 0.1U 0402 +80-20% 16V
C144 0.1U 0402 +80-20% 16V
C150 1000P 0402 10% 50V
R175 33 0402 HCLK_CPU
R176 33 0402 HCLK_CPU#
R173 33 0402 HCLK_SISM661FX
R174 33 0402 HCLK_SISM661FX#
R179 22 0402 AGP_CLK
R214 22 0402 ZCLK0
R215 22 0402 ZCLK1
FS3
FS4
R217 33 0402 CLK_SBPCI
R219 33 0402 PCI_KBCLK
R220 33 0402 PCICLK_CARD
R221 33 0402 PCICLK_FWH
R206 33 0402 CLK_MINIPCI
R200 33 0402 14.318MHZ_TV
R201 33 0402 REFCLK0
R212 33 0402 REFCLK1
FS0
FS2
R190 10K 0402
R194 22 0402 USB12M_SB
R186 22 0402 USBCLK_SB
R180 22 0402 CLK_SIO
ASMBCLK
ASMBDATA
HCLK_CPU [4]
HCLK_CPU# [4]
HCLK_SISM661FX [6]
HCLK_SISM661FX# [6]
AGP_CLK [6]
ZCLK0 [6]
ZCLK1 [12]
CLK_SBPCI [12]
PCI_KBCLK [20]
PCICLK_CARD [16]
PCICLK_FWH [18]
CLK_MINIPCI [21]
14.318MHZ_TV [8]
REFCLK0 [6]
REFCLK1 [13]
USB12M_SB [14]
USBCLK_SB [14]
CLK_SIO [21]
+12VS
R133 10K 0402 5%
Q16 2N7002
Q12 2N7002
SMBCLK
SMBDATA
SMBCLK [9,13]
SMBDATA [9,13]
R181 10K 0402 5%
SMBus address: D2h by BIOS
R178 4.7K 0402
R177 4.7K 0402
Layout note: Place crystal within 500 mils of CLK Gen.
X3
14.31818MHZ
C195 22P 0603 5%
C196 22P 0603 5%
SMBus address: D4h by BIOS
VDD_MEM2.5
L61 120Z/100M
L60 120Z/100M
C254 0.1U 0402 +80-20% 16V
C233 0.1U 0402 +80-20% 16V
C253 0.1U 0402 +80-20% 16V
C255 1000P 0402 10% 50V
[6] FWDSDCLKO
BF_OUT
FWDSDCLKO
U19
SCLK
SDATA
FBINT
CLK_INT
VDD0
VDD1
VDD2
VDDA
GND0
GND1
GND2
GND3
N/C0
N/C1
N/C2
ICS93772
SSOP28A
FB_OUTT
CLKT0
CLKC0
CLKT1
CLKC1
CLKT2
CLKC2
CLKT3
CLKC3
CLKT4
CLKC4
CLKT5
CLKC5
R256 22 0402
R279 0_DFS 0402 CLK_DDR0
R278 0_DFS 0402 CLK_DDR0#
R281 0_DFS 0402 CLK_DDR1
R282 0_DFS 0402 CLK_DDR1#
R284 0_DFS 0402 CLK_DDR2
R285 0_DFS 0402 CLK_DDR2#
R253 0_DFS 0402 CLK_DDR3
R254 0_DFS 0402 CLK_DDR3#
R252 0_DFS 0402 CLK_DDR4
R251 0_DFS 0402 CLK_DDR4#
R249 0_DFS 0402 CLK_DDR5
R258 0_DFS 0402 CLK_DDR5#
CLK_DDR0 [9]
CLK_DDR0# [9]
CLK_DDR1 [9]
CLK_DDR1# [9]
CLK_DDR2 [9]
CLK_DDR2# [9]
CLK_DDR3 [9]
CLK_DDR3# [9]
CLK_DDR4 [9]
CLK_DDR4# [9]
CLK_DDR5 [9]
CLK_DDR5# [9]
PLACE AT CLK SIDE
R209 10K/NA 0402
R218 10K/NA 0402
R227 1K 0402 1%
R226 1K 0402 1%
FS0
FS4
FS3
R216 10K 0402
BSEL1
FS2
R213 10K 0402
BSEL0
BSEL1 [4]
BSEL0 [4]
HCLK_SISM661FX
HCLK_SISM661FX#
HCLK_CPU
HCLK_CPU#
R164 49.9 0402 1%
R165 49.9 0402 1%
R166 49.9 0402 1%
R167 49.9 0402 1%
R0C
C31 10P 0402
C30 10P 0402
C147 10P/NA 0402
C139 10P/NA 0402
C229 10P 0402

For ICS952011

Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	0	100.20	100.20	66.8	66.8	33.4
0	0	0	0	1	100.20	133.60	66.8	66.8	33.4
0	0	0	1	0	100.20	200.4	66.8	66.8	33.4
0	0	0	1	1	100.20	167.00	66.8	66.8	33.4
0	0	1	0	0	133.60	100.20	66.8	66.8	33.4
0	0	1	0	1	133.60	133.60	66.8	66.8	33.4
0	0	1	1	0	133.60	200.40	66.8	66.8	33.4
0	0	1	1	1	133.60	167.00	66.8	66.8	33.4
0	1	0	0	0	200.05	100.03	66.68	66.68	33.34
0	1	0	0	1	200.05	133.37	66.68	66.68	33.34
0	1	0	1	0	200.05	200.05	66.68	66.68	33.34
0	1	0	1	1	200.05	160.04	66.68	66.68	33.34
0	1	1	0	0	166.70	100.20	66.68	66.68	33.34
0	1	1	0	1	166.70	133.36	66.8	66.8	33.4
0	1	1	1	0	160.04	200.05	66.68	66.68	33.34
0	1	1	1	1	166.7	166.7	66.68	66.68	33.34
1	0	0	0	0	100.20	100.02	133.60	66.8	33.4
1	0	0	0	1	100.20	133.60	133.60	66.8	33.4
1	0	0	1	0	100.20	200.40	133.60	66.8	33.4
1	0	0	1	1	100.20	167.00	133.60	66.8	33.4
1	0	1	0	0	133.60	100.20	133.60	66.8	33.4
1	0	1	0	1	133.60	133.60	133.60	66.8	33.4
1	0	1	1	0	133.60	200.40	133.60	66.8	33.4
1	0	1	1	1	133.60	167.00	133.60	66.8	33.4
1	1	0	0	0	200.05	100.03	133.37	66.68	33.34
1	1	0	0	1	200.05	133.37	133.37	66.68	33.34
1	1	0	1	0	200.05	200.05	133.37	66.68	33.34
1	1	0	1	1	200.05	160.04	133.37	66.68	33.34
1	1	1	0	0	166.70	100.20	133.60	66.68	33.4
1	1	1	0	1	166.70	133.36	133.60	66.8	33.4
1	1	1	1	0	160.04	200.05	133.37	66.68	33.34
1	1	1	1	1	166.70	166.70	133.37	66.68	33.34

NON USE

BSEL1	BSEL0	FREQ
L	L	100MHz
L	H	133MHz
H	L	200MHz
H	H	RSVD

☐ **DEFAULT**

For ICS952007

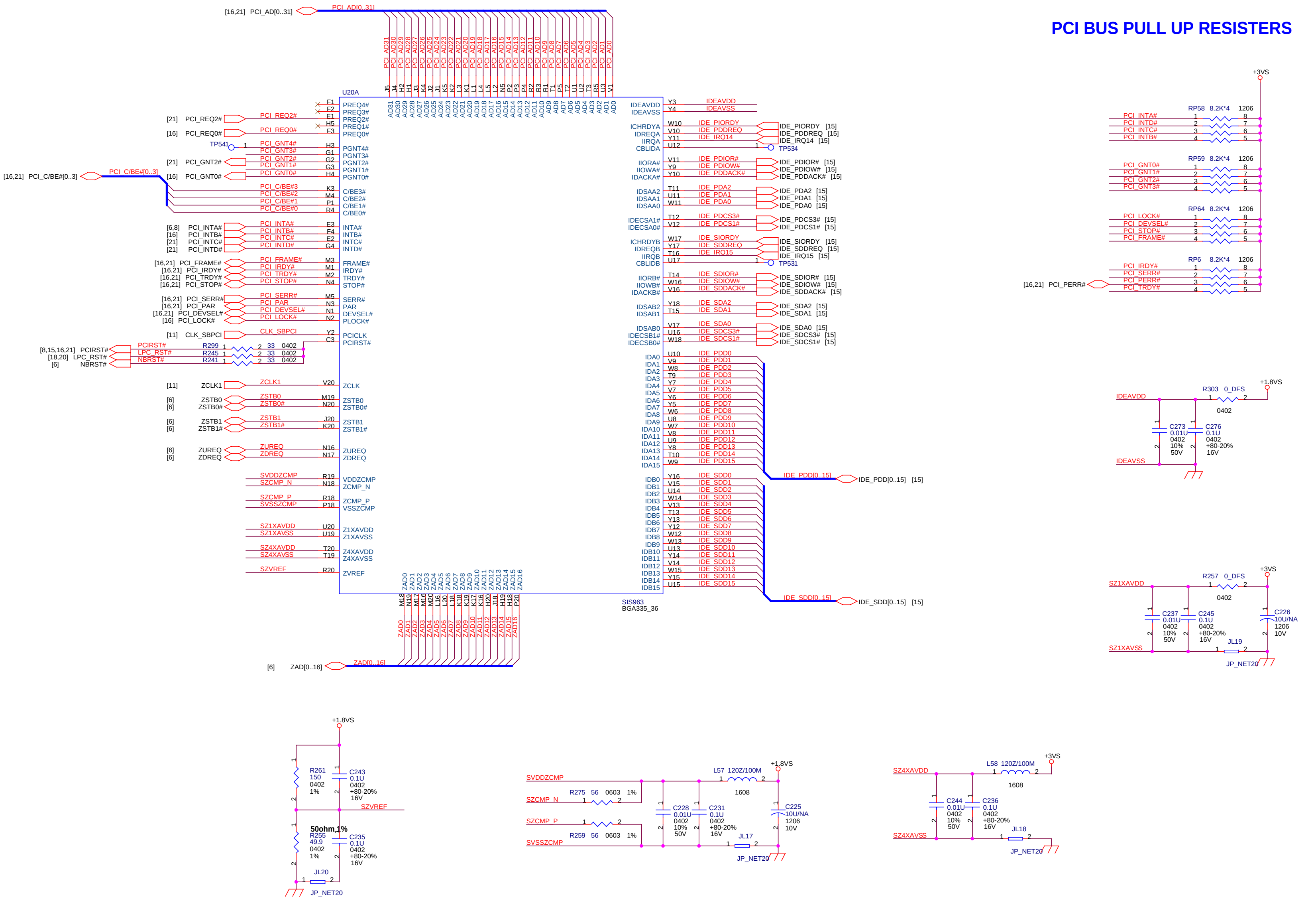
Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	SDRAM	ZCLK	AGP	PCI
0	0	0	0	0	100.00	100.00	133.33	66.66	33.33
0	0	0	0	1	100.99	133.99	134.65	67.33	33.66
0	0	0	1	0	103.00	103.00	137.33	68.67	34.33
0	0	0	1	1	100.00	100.00	133.33	66.67	33.33
0	0	1	0	0	133.33	133.33	133.33	66.66	33.33
0	0	1	0	1	134.65	134.65	134.65	67.32	33.66
0	0	1	1	0	137.33	137.33	137.33	68.66	34.33
0	0	1	1	1	133.33	133.33	133.33	66.67	33.33
0	1	0	0	0	200.00	200.00	133.33	66.67	33.33
0	1	0	0	1	201.98	201.98	134.65	67.33	33.66
0	1	0	1	0	206.00	206.00	137.33	68.67	34.33
0	1	0	1	1	200.00	200.00	133.33	66.67	33.33
0	1	1	0	0	166.66	166.66	133.33	66.66	33.33
0	1	1	0	1	168.31	168.31	134.65	67.32	33.66
0	1	1	1	0	171.66	171.66	137.33	68.66	34.33
0	1	1	1	1	166.66	166.66	133.33	66.66	33.33
1	0	0	0	0	100.20	100.02	133.60	66.79	33.40
1	0	0	0	1	105.00	105.00	140.00	69.99	35.00
1	0	0	1	0	107.00	107.00	142.66	71.33	35.66
1	0	0	1	1	110.00	110.00	146.66	73.33	36.66
1	0	1	0	0	133.60	133.60	133.60	66.79	33.40
1	0	1	0	1	140.00	140.00	140.00	69.99	35.00
1	0	1	1	0	142.66	142.66	142.66	71.33	35.66
1	0	1	1	1	146.66	146.66	146.66	73.33	36.66
1	1	0	0	0	200.40	200.40	133.60	66.79	33.40
1	1	0	0	1	210.00	210.00	140.00	69.99	35.00
1	1	0	1	0	214.00	214.00	142.66	71.33	35.66
1	1	0	1	1	220.00	220.00	146.66	73.33	36.66
1	1	1	0	0	166.99	166.99	133.60	66.79	33.40
1	1	1	0	1	174.99	174.99	140.00	69.99	35.00
1	1	1	1	0	178.33	178.33	142.66	71.33	35.66
1	1	1	1	1	183.33	183.33	146.66	73.33	36.66

NON USE

MiTAC

Title
Clock Generator/Buffer
Size
Document Number **411682900001**
Rev R06
Date: Monday, April 12, 2004
Sheet 11 of 28

SIS963L (1/3)



PCI BUS PULL UP RESISTERS
U20A
SIS963
BGA335_36
[16,21] PCI_AD[0..31]
PCI_AD[0..31]
[21] PCI_REQ2#
[16] PCI_REQ0#
TP541
[21] PCI_GNT2#
[16] PCI_GNT0#
[16,21] PCI_C/BE#[0..3]
PCI_C/BE#[0..3]
[6,8] PCI_INTA#
[16] PCI_INTB#
[21] PCI_INTC#
[21] PCI_INTD#
[16,21] PCI_FRAME#
[16,21] PCI_IRDY#
[16,21] PCI_TRDY#
[16,21] PCI_STOP#
[16,21] PCI_SERR#
[16,21] PCI_PAR
[16,21] PCI_DEVSEL#
[16] PCI_LOCK#
[11] CLK_SBPCI
[8,15,16,21] PCIRST#
[18,20] LPC_RST#
[6] NBRST#
R299 33 0402
R245 33 0402
R241 33 0402
[11] ZCLK1
[6] ZSTB0
[6] ZSTB0#
[6] ZSTB1
[6] ZSTB1#
[6] ZUREQ
[6] ZDREQ
SVDDZCMP
SZCMP_N
SZCMP_P
SVSSZCMP
SZ1XAVDD
SZ1XAVSS
SZ4XAVDD
SZ4XAVSS
SZVREF
[6] ZAD[0..16]
ZAD[0..16]
IDEAVDD
IDEAVSS
IDE_PIORDY [15]
IDE_PDDREQ [15]
IDE_IRQ14 [15]
TP534
IDE_PDIOR# [15]
IDE_PDIOW# [15]
IDE_PDDACK# [15]
IDE_PDA2 [15]
IDE_PDA1 [15]
IDE_PDA0 [15]
IDE_PDCS3# [15]
IDE_PDCS1# [15]
IDE_SIORDY [15]
IDE_SDDREQ [15]
IDE_IRQ15 [15]
TP531
IDE_SDIOR# [15]
IDE_SDIOW# [15]
IDE_SDDACK# [15]
IDE_SDA2 [15]
IDE_SDA1 [15]
IDE_SDA0 [15]
IDE_SDCS3# [15]
IDE_SDCS1# [15]
IDE_PDD[0..15] [15]
IDE_SDD[0..15] [15]
+3VS
RP58 8.2K*4 1206
RP59 8.2K*4 1206
RP64 8.2K*4 1206
RP6 8.2K*4 1206
[16,21] PCI_PERR#
+1.8VS
R303 0_DFS 0402
C273 0.01U 0402 10% 50V
C276 0.1U 0402 +80-20% 16V
R257 0_DFS 0402
C237 0.01U 0402 10% 50V
C245 0.1U 0402 +80-20% 16V
C226 10U/NA 1206 10V
JL19 JP_NET20
R261 150 0402 1%
C243 0.1U 0402 +80-20% 16V
50ohm 1%
R255 49.9 0402 1%
C235 0.1U 0402 +80-20% 16V
JL20 JP_NET20
L57 120Z/100M 1608
R275 56 0603 1%
R259 56 0603 1%
C228 0.01U 0402 10% 50V
C231 0.1U 0402 +80-20% 16V
C225 10U/NA 1206 10V
JL17 JP_NET20
L58 120Z/100M 1608
C244 0.01U 0402 10% 50V
C236 0.1U 0402 +80-20% 16V
JL18 JP_NET20

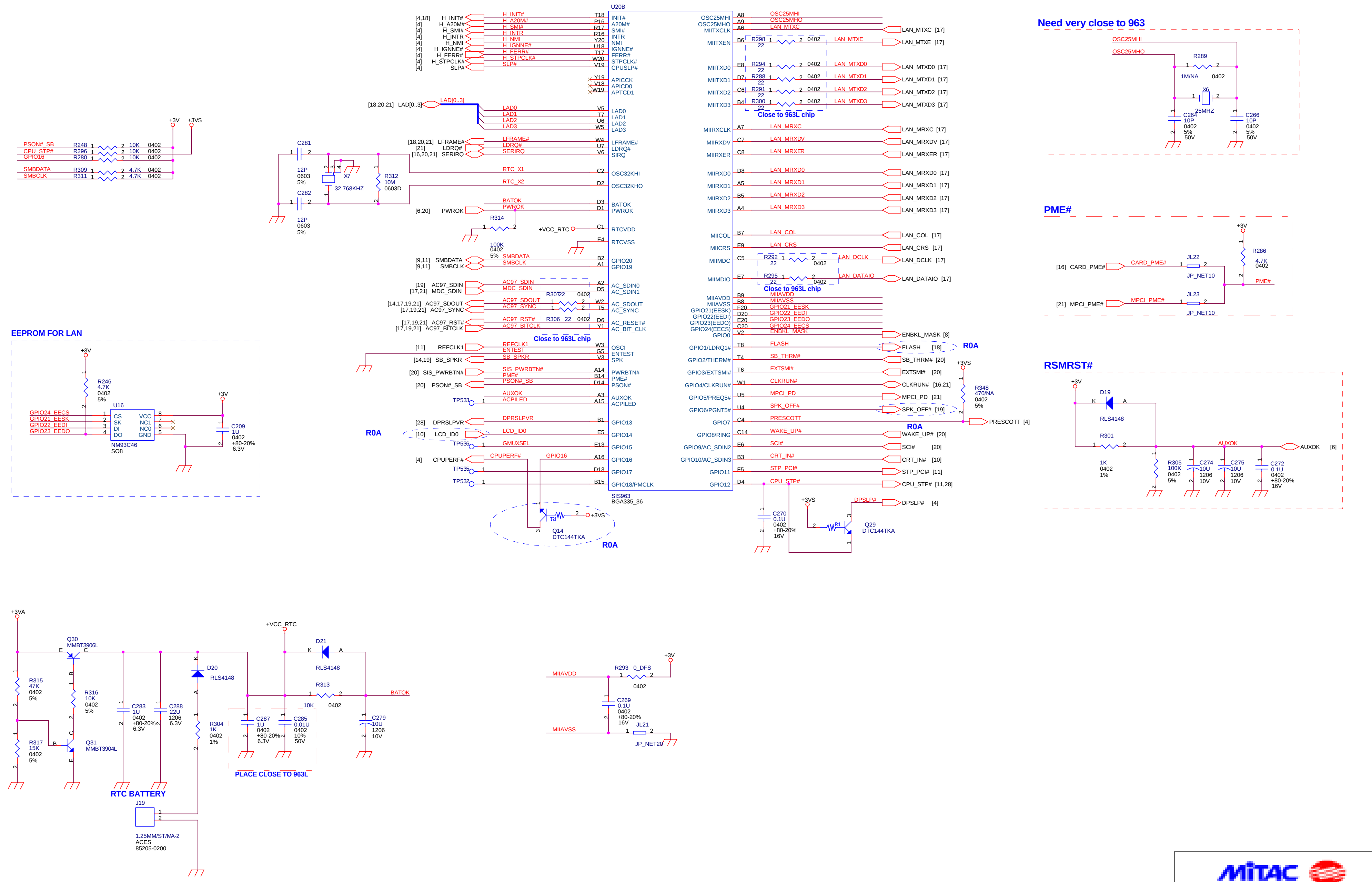
MiTAC

Title
SIS963 (1/3)

Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 12 of 28

SIS963L (2/3)


U20B
SIS963
BGA335_36
[4,18] H_INIT# T18 INIT#
[4] H_A20M# P16 A20M#
[4] H_SMI# R17 SMI#
[4] H_INTR R16 INTR
[4] H_NMI Y20 NMI
[4] H_IGNNE# U18 IGNNE#
[4] H_FERR# T17 FERR#
[4] H_STPCLK# W20 STPCLK#
[4] SLP# V19 CPUSLP#
Y19 APICCK
V18 APICD0
W19 APTCD1
[18,20,21] LAD[0..3]
LAD0 V5 LAD0
LAD1 T7 LAD1
LAD2 U6 LAD2
LAD3 W5 LAD3
[18,20,21] LFRAME# W4 LFRAME#
[21] LDRQ# U7 LDRQ#
[16,20,21] SERIRQ V6 SIRQ
RTC_X1 C2 OSC32KHI
RTC_X2 D2 OSC32KHO
BATOK D3 BATOK
[6,20] PWROK D1 PWROK
+VCC_RTC C1 RTCVDD
E4 RTCVSS
[9,11] SMBDATA B2 GPIO20
[9,11] SMBCLK A1 GPIO19
[19] AC97_SDIN A2 AC_SDIN0
[17,21] MDC_SDIN D5 AC_SDIN1
[14,17,19,21] AC97_SDOUT W2 AC_SDOUT
[17,19,21] AC97_SYNC T5 AC_SYNC
[17,19,21] AC97_RST# D6 AC_RESET#
[17,19,21] AC97_BITCLK Y1 AC_BIT_CLK
R307 22 0402
R306 22 0402
Close to 963L chip
[11] REFCLK1 W3 OSCI
ENTEST G5 ENTEST
[14,19] SB_SPKR V3 SPK
[20] SIS_PWRBTN# A14 PWRBTN#
PME# B14 PME#
[20] PSON#_SB D14 PSON#
TP533 AUXOK A3 AUXOK
ACPILED A15 ACPILED
[28] DPRSLPVR B1 GPIO13
[10] LCD_ID0 E5 GPIO14
TP536 GMUXSEL E13 GPIO15
[4] CPUPERF# GPIO16 A16 GPIO16
TP535 D13 GPIO17
TP532 B15 GPIO18/PMCLK
R0A
Q14 DTC144TKA
+3VS
R0A
OSC25MHI A8 OSC25MHI
OSC25MHO A9 OSC25MHO
LAN_MTXC A6 MIITXCLK LAN_MTXC [17]
R298 22 0402 B6 MIITXEN LAN_MTXE [17]
R294 22 0402 E8 MIITXD0 LAN_MTXD0 [17]
R288 22 0402 D7 MIITXD1 LAN_MTXD1 [17]
R291 22 0402 C6 MIITXD2 LAN_MTXD2 [17]
R300 22 0402 B4 MIITXD3 LAN_MTXD3 [17]
Close to 963L chip
A7 MIIRXCLK LAN_MRXC [17]
C7 MIIRXDV LAN_MRXDV [17]
C8 MIIRXER LAN_MRXER [17]
D8 MIIRXD0 LAN_MRXD0 [17]
A5 MIIRXD1 LAN_MRXD1 [17]
B5 MIIRXD2 LAN_MRXD2 [17]
A4 MIIRXD3 LAN_MRXD3 [17]
B7 MIICOL LAN_COL [17]
E9 MIICRS LAN_CRS [17]
R292 22 0402 C5 MIIMDC LAN_DCLK [17]
R295 22 0402 E7 MIIMDIO LAN_DATAIO [17]
Close to 963L chip
B9 MIIAVDD
B8 MIIAVSS
F20 GPIO21(EESK)
D20 GPIO22(EEDI)
E20 GPIO23(EEDO)
C20 GPIO24(EECS)
V2 GPIO0 ENBKL_MASK [8]
T8 GPIO1/LDRQ1# FLASH [18]
T4 GPIO2/THERM# SB_THRM# [20]
T6 GPIO3/EXTSMI# EXTSMI# [20]
W1 GPIO4/CLKRUN# CLKRUN# [16,21]
U5 GPIO5/PREQ5# MPCI_PD [21]
U4 GPIO6/PGNT5# SPK_OFF# [19]
C4 GPIO7 PRESCOTT PRESCOTT [4]
C14 GPIO8/RING WAKE_UP# [20]
E6 GPIO9/AC_SDIN2 SCI# [20]
B3 GPIO10/AC_SDIN3 CRT_IN# [10]
F5 GPIO11 STP_PCI# [11]
D4 GPIO12 CPU_STP# [11,28]
R0A
R0A
+3VS
R348 470/NA 0402 5%
C270 0.1U 0402 +80-20% 16V
DPSLP# [4]
Q29 DTC144TKA
PSON#_SB R248 10K 0402
CPU_STP# R296 10K 0402
GPIO16 R280 10K 0402
SMBDATA R309 4.7K 0402
SMBCLK R311 4.7K 0402
+3V +3VS
C281 12P 0603 5%
C282 12P 0603 5%
X7 32.768KHZ
R312 10M 0603D
R314
Need very close to 963
OSC25MHI
OSC25MHO
R289 1M/NA 0402
X6 25MHZ
C264 10P 0402 5% 50V
C266 10P 0402 5% 50V
PME#
+3V
R286 4.7K 0402
[16] CARD_PME# JL22 JP_NET10
[21] MPCI_PME# JL23 JP_NET10
PME#
RSMRST#
+3V
D19 RLS4148
R301 1K 0402 1%
R305 100K 0402 5%
C274 10U 1206 10V
C275 10U 1206 10V
C272 0.1U 0402 +80-20% 16V
AUXOK AUXOK [6]
EEPROM FOR LAN
+3V
R246 4.7K 0402 5%
U16 NM93C46 SO8
GPIO24_EECS 1 CS VCC 8
GPIO21_EESK 2 SK NC1 7
GPIO22_EEDI 3 DI NC0 6
GPIO23_EEDO 4 DO GND 5
+3V
C209 1U 0402 +80-20% 6.3V
+3VA
Q30 MMBT3906L
R315 47K 0402 5%
R316 10K 0402 5%
R317 15K 0402 5%
Q31 MMBT3904L
C283 1U 0402 +80-20% 6.3V
C288 22U 1206 6.3V
D20 RLS4148
R304 1K 0402 1%
RTC BATTERY
J19 1.25MM/ST/MA-2 ACES 85205-0200
+VCC_RTC
D21 RLS4148
R313 10K 0402
BATOK
C287 1U 0402 +80-20% 6.3V
C285 0.01U 0402 10% 50V
C279 10U 1206 10V
PLACE CLOSE TO 963L
+3V
MIIAVDD R293 0_DFS 0402
C269 0.1U 0402 +80-20% 16V
MIIAVSS JL21 JP_NET20

MiTAC

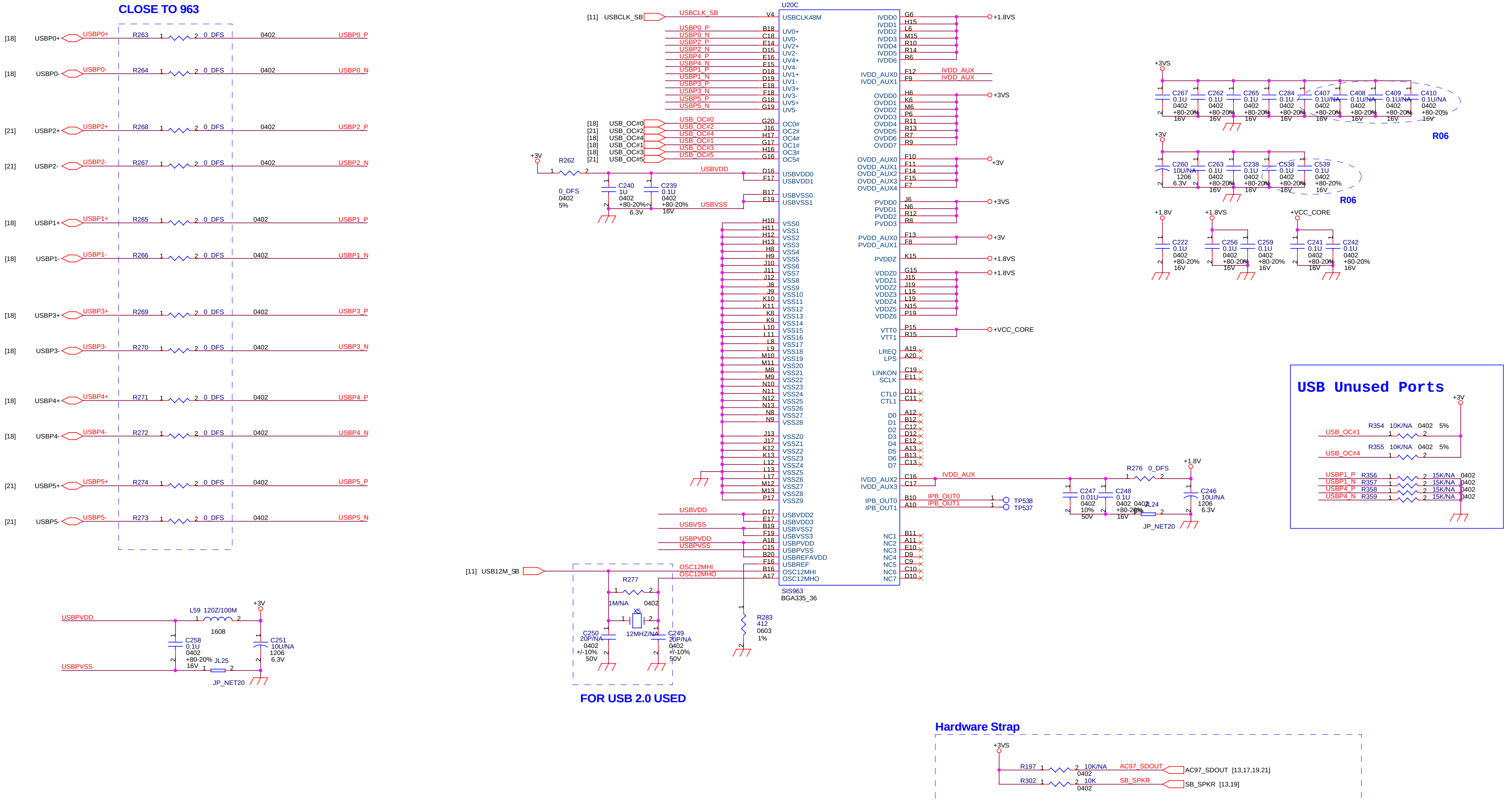
Title
SIS963 (2/3)

Size
Document Number
411682900001

Rev
R06

Date: Monday, April 12, 2004
Sheet 13 of 28

SIS963L (3/3)

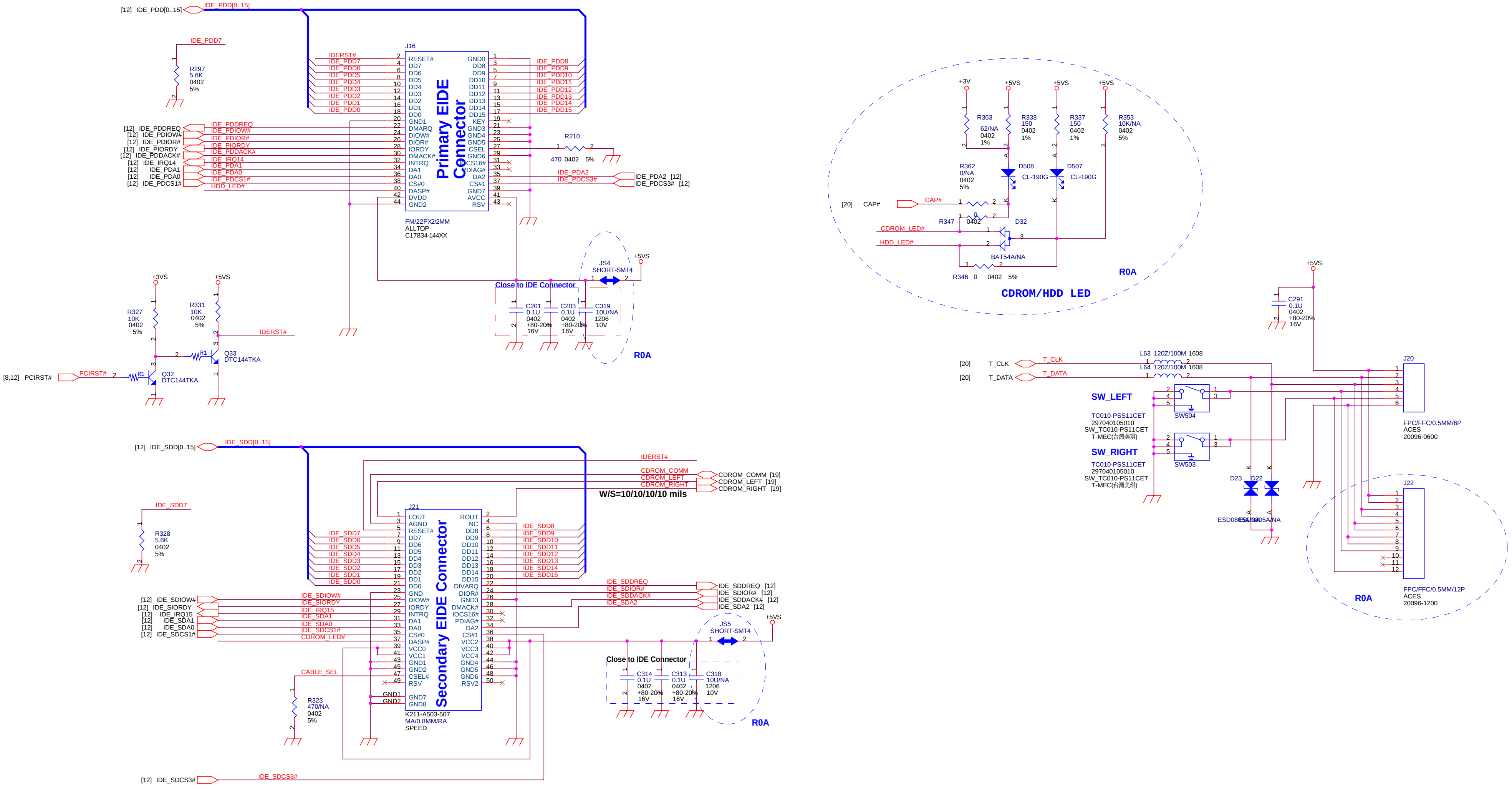

CLOSE TO 963
USBP0+ USBP0- USBP2+ USBP2- USBP1+ USBP1- USBP3+ USBP3- USBP4+ USBP4- USBP5+ USBP5-
R263 R264 R268 R267 R265 R266 R269 R270 R271 R272 R274 R273 0_DFS 0402
USBP0_P USBP0_N USBP2_P USBP2_N USBP1_P USBP1_N USBP3_P USBP3_N USBP4_P USBP4_N USBP5_P USBP5_N
U20C
USBCLK48M
USBCLK_SB
USB_OC#0 USB_OC#2 USB_OC#4 USB_OC#1 USB_OC#3 USB_OC#5
USBVDD USBVSS USBPVDD USBPVSS
OSC12MHI OSC12MHO
USB12M_SB
SIS963
BGA335_36
IVDD_AUX
IPB_OUT0 IPB_OUT1
TP538 TP537
JP_NET20
+1.8VS +3VS +3V +1.8V +VCC_CORE
R06
FOR USB 2.0 USED
L59 120Z/100M
C258 C251
R277 1M/NA
X5 12MHZ/NA
C250 20P/NA C249 20P/NA
R283 412 0603 1%
USB Unused Ports
R354 10K/NA 0402 5%
R355 10K/NA 0402 5%
R356 R357 R358 R359 15K/NA 0402
Hardware Strap
R197 10K/NA 0402
R302 10K 0402
AC97_SDOUT [13,17,19,21]
SB_SPKR [13,19]

Symbol	0	1	Default	Notes
SB_SPKR (LPC addr mapping)	**disable**	**enable**	**0**	**Internal Pull-down**
AC97_SDOUT (Trap mode)	**ROM**	**Reserved**	**0**	**Internal Pull-down**
USB_OC4# (South bridge debug mode)	**enable**	**disable**	**1**	
IPB_OUT0(MuTIOL clock PLL)	**enable**	**disable**	**0**	**Internal Pull-down**
IPB_OUT1(MuTIOL operation mode select)	**Full-swing**	**Partial-swing**	**0**	**Internal Pull-down**
AC97_SYNC (PCICLK PLL)	**enable**	**disable**	**0**	**Internal Pull-down**

MiTAC

Title
SIS963L (3/3)
Size
Document Number 411682900001
Rev R06
Date: Monday, April 12, 2004
Sheet 14 of 28

IDE Interface



[12] IDE_PDD[0..15]
IDE_PDD[0..15]
IDE_PDD7
R297 5.6K 0402 5%
J16
Primary EIDE Connector
RESET#
DD7
DD6
DD5
DD4
DD3
DD2
DD1
DD0
GND1
DMARQ
DIOW#
DIOR#
IORDY
DMACK#
INTRQ
DA1
DA0
CS#0
DASP#
DVDD
GND2
GND0
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
KEY
GND3
GND4
GND5
CSEL
GND6
IOCS16#
PDIAG#
DA2
CS#1
GND7
AVCC
RSV
IDERST#
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
[12] IDE_PDDREQ
[12] IDE_PDIOW#
[12] IDE_PDIOR#
[12] IDE_PIORDY
[12] IDE_PDDACK#
[12] IDE_IRQ14
[12] IDE_PDA1
[12] IDE_PDA0
[12] IDE_PDCS1#
HDD_LED#
R210 470 0402 5%
IDE_PDA2 [12]
IDE_PDCS3# [12]
FM/22PX2/2MM
ALLTOP
C17834-144XX
JS4 SHORT-SMT4
+5VS
Close to IDE Connector
C201 0.1U 0402 +80-20% 16V
C203 0.1U 0402 +80-20% 16V
C319 10U/NA 1206 10V
R0A
+3VS
+5VS
R327 10K 0402 5%
R331 10K 0402 5%
IDERST#
Q33 DTC144TKA
[8,12] PCIRST#
PCIRST#
Q32 DTC144TKA
+3V
+5VS
+5VS
+5VS
R363 62/NA 0402 1%
R338 150 0402 1%
R337 150 0402 1%
R353 10K/NA 0402 5%
R362 0/NA 0402 5%
D508 CL-190G
D507 CL-190G
[20] CAP#
CAP#
R347 0 0402
D32
CDROM_LED#
HDD_LED#
BAT54A/NA
R346 0 0402 5%
R0A
CDROM/HDD LED
+5VS
C291 0.1U 0402 +80-20% 16V
[20] T_CLK
[20] T_DATA
T_CLK
T_DATA
L63 120Z/100M 1608
L64 120Z/100M 1608
J20
SW_LEFT
SW504
TC010-PSS11CET
297040105010
SW_TC010-PS11CET
T-MEC(台灣美琪)
SW_RIGHT
SW503
TC010-PSS11CET
297040105010
SW_TC010-PS11CET
T-MEC(台灣美琪)
FPC/FFC/0.5MM/6P
ACES
20096-0600
D23 D22
ESD0805V05A/NA
J22
FPC/FFC/0.5MM/12P
ACES
20096-1200
R0A
[12] IDE_SDD[0..15]
IDE_SDD[0..15]
IDERST#
CDROM_COMM
CDROM_LEFT
CDROM_RIGHT
CDROM_COMM [19]
CDROM_LEFT [19]
CDROM_RIGHT [19]
W/S=10/10/10/10 mils
IDE_SDD7
R328 5.6K 0402 5%
J21
Secondary EIDE Connector
LOUT
AGND
RESET#
DD7
DD6
DD5
DD4
DD3
DD2
DD1
DD0
GND
DIOW#
IORDY
INTRQ
DA1
DA0
CS#0
DASP#
VCC0
VCC1
GND1
GND2
CSEL#
RSV
ROUT
NC
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DIVARQ
DIOR#
GND3
DMACK#
IOCS16#
PDIAG#
DA2
CS#1
VCC2
VCC3
VCC4
GND4
GND5
GND6
RSV2
GND7
GND8
K211-A503-507
MA/0.8MM/RA
SPEED
IDE_SDD8
IDE_SDD9
IDE_SDD10
IDE_SDD11
IDE_SDD12
IDE_SDD13
IDE_SDD14
IDE_SDD15
IDE_SDDREQ
IDE_SDIOR#
IDE_SDDACK#
IDE_SDA2
IDE_SDDREQ [12]
IDE_SDIOR# [12]
IDE_SDDACK# [12]
IDE_SDA2 [12]
[12] IDE_SDIOW#
[12] IDE_SIORDY
[12] IDE_IRQ15
[12] IDE_SDA1
[12] IDE_SDA0
[12] IDE_SDCS1#
CDROM_LED#
CABLE_SEL
R323 470/NA 0402 5%
GND1
GND2
+5VS
JS5 SHORT-SMT4
Close to IDE Connector
C314 0.1U 0402 +80-20% 16V
C313 0.1U 0402 +80-20% 16V
C318 10U/NA 1206 10V
R0A
[12] IDE_SDCS3#
IDE_SDCS3#

MiTAC

Title

IDE INTERFACE & IR

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 15 of 28

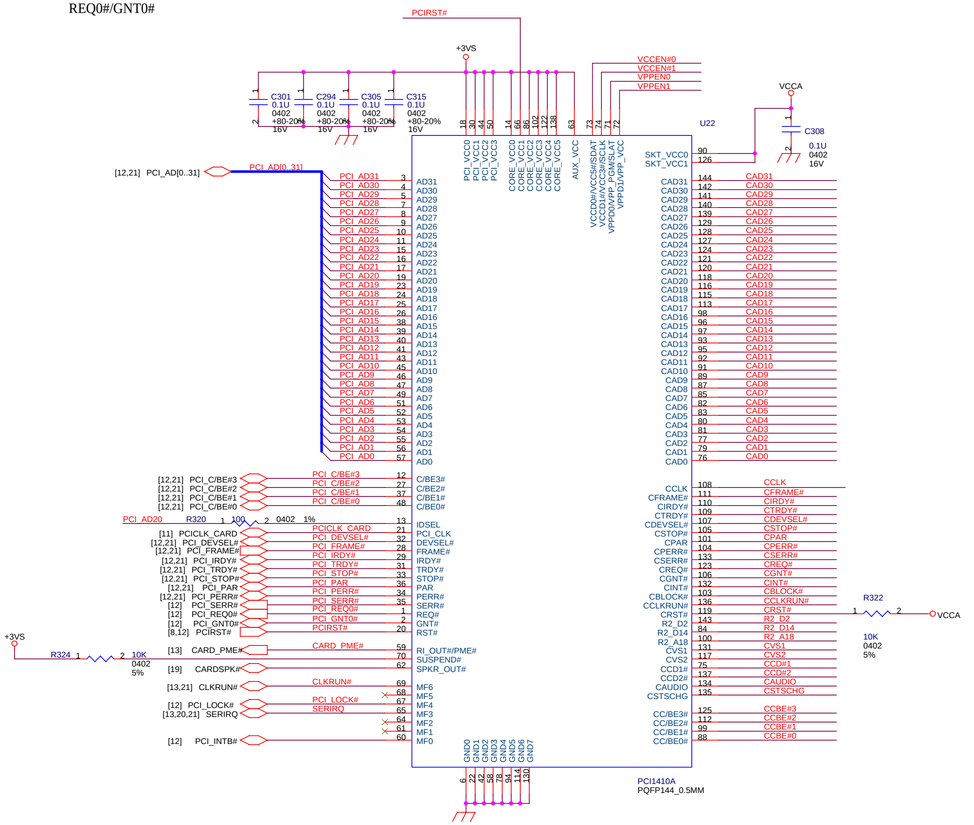
PCMCIA (Ti PCI1410A)

PCMCIA CONTROLLER & CARDBUS SCOKET

AD20

PCI_INTB#

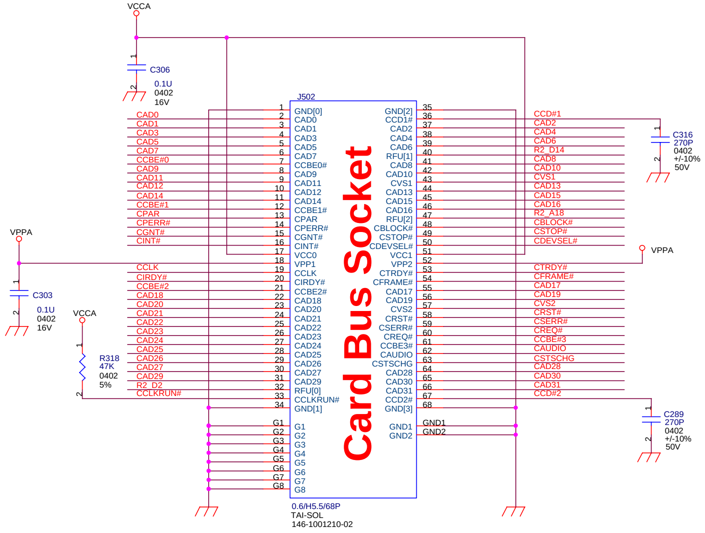
REQ0#/GNT0#

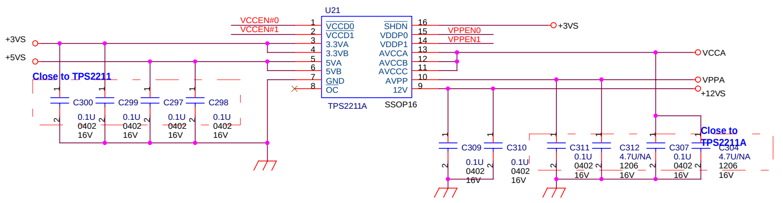

PCIRST#
+3VS
C301 0.1U 0402 +80-20% 16V
C294 0.1U 0402 +80-20% 16V
C305 0.1U 0402 +80-20% 16V
C315 0.1U 0402 +80-20% 16V
VCCEN#0
VCCEN#1
VPPEN0
VPPEN1
VCCA
C308 0.1U 0402 16V
U22
PCI_VCC0 PCI_VCC1 PCI_VCC2 PCI_VCC3
CORE_VCC0 CORE_VCC1 CORE_VCC2 CORE_VCC3 CORE_VCC4 CORE_VCC5
AUX_VCC
VCCD0#/VCC5#/SDAT
VCCD1#/VCC3#/SCLK
VPPD0/VPP_PGM/SLAT
VPPD1/VPP_VCC
SKT_VCC0
SKT_VCC1
[12,21] PCI_AD[0..31]
PCI_AD[0..31]
PCI_AD31 … PCI_AD0
AD31 … AD0
CAD31 … CAD0
[12,21] PCI_C/BE#3
[12,21] PCI_C/BE#2
[12,21] PCI_C/BE#1
[12,21] PCI_C/BE#0
C/BE3# C/BE2# C/BE1# C/BE0#
PCI_AD20
R320 100 0402 1%
IDSEL
[11] PCICLK_CARD
[12,21] PCI_DEVSEL#
[12,21] PCI_FRAME#
[12,21] PCI_IRDY#
[12,21] PCI_TRDY#
[12,21] PCI_STOP#
[12,21] PCI_PAR
[12,21] PCI_PERR#
[12] PCI_SERR#
[12] PCI_REQ0#
[12] PCI_GNT0#
[8,12] PCIRST#
PCI_CLK DEVSEL# FRAME# IRDY# TRDY# STOP# PAR PERR# SERR# REQ# GNT# RST#
+3VS
R324 10K 0402 5%
[13] CARD_PME#
[19] CARDSPK#
RI_OUT#/PME#
SUSPEND#
SPKR_OUT#
[13,21] CLKRUN#
[12] PCI_LOCK#
[13,20,21] SERIRQ
[12] PCI_INTB#
MF6 MF5 MF4 MF3 MF2 MF1 MF0
CCLK CFRAME# CIRDY# CTRDY# CDEVSEL# CSTOP# CPAR CPERR# CSERR# CREQ# CGNT# CINT# CBLOCK# CCLKRUN# CRST# R2_D2 R2_D14 R2_A18 CVS1 CVS2 CCD1# CCD2# CAUDIO CSTSCHG
CC/BE3# CC/BE2# CC/BE1# CC/BE0#
CCBE#3 CCBE#2 CCBE#1 CCBE#0
R322 10K 0402 5%
VCCA
GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7
PCI1410A
PQFP144_0.5MM

SIGNAL PC CARD PULL UP VOLT

SIGNAL	PC CARD PULL UP	VOLT
CCD#1	+3V	
CCD#2	+3V	
CBLOCK#	CARD_VCC	
CSTOP#	CARD_VCC	
CDEVSEL#	CARD_VCC	
CTRDY#	CARD_VCC	
CVS1	+3V	
CVS2	+3V	
CRST#	CARD_VCC	
CSERR#	CARD_VCC	
CPERR#	CARD_VCC	
CINT#	CARD_VCC	
CIRDY#	CARD_VCC	
CREQ#	CARD_VCC	
CSTSCHG#	CARD_VCC	
CAUDIO	CARD_VCC	

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE


VCCA
C306 0.1U 0402 16V
J502
Card Bus Socket
GND[0] CAD0 CAD1 CAD3 CAD5 CAD7 CCBE0# CAD9 CAD11 CAD12 CAD14 CCBE1# CPAR CPERR# CGNT# CINT# VCC0 VPP1 CCLK CIRDY# CCBE2# CAD18 CAD20 CAD21 CAD22 CAD23 CAD24 CAD25 CAD26 CAD27 CAD29 RFU[0] CCLKRUN# GND[1]
GND[2] CCD1# CAD2 CAD4 CAD6 RFU[1] CAD8 CAD10 CVS1 CAD13 CAD15 CAD16 RFU[2] CBLOCK# CSTOP# CDEVSEL# VCC1 VPP2 CTRDY# CFRAME# CAD17 CAD19 CVS2 CRST# CSERR# CREQ# CCBE3# CAUDIO CSTSCHG CAD28 CAD30 CAD31 CCD2# GND[3]
G1 G2 G3 G4 G5 G6 G7 G8
GND1 GND2
VPPA
C303 0.1U 0402 16V
VCCA
R318 47K 0402 5%
C316 270P 0402 +/-10% 50V
C289 270P 0402 +/-10% 50V
VPPA
0.6/H5.5/68P
TAI-SOL
146-1001210-02


U21
VCCEN#0
VCCEN#1
+3VS
+5VS
Close to TPS2211
C300 0.1U 0402 16V
C299 0.1U 0402 16V
C297 0.1U 0402 16V
C298 0.1U 0402 16V
VCCD0 VCCD1 3.3VA 3.3VB 5VA 5VB GND OC
SHDN VDDP0 VDDP1 AVCCA AVCCB AVCCC AVPP 12V
TPS2211A SSOP16
VPPEN0
VPPEN1
+3VS
VCCA
VPPA
+12VS
C309 0.1U 0402 16V
C310 0.1U 0402 16V
C311 0.1U 0402 16V
C312 4.7U/NA 1206 16V
C307 0.1U 0402 16V
C304 4.7U/NA 1206 16V
Close to TPS2211A

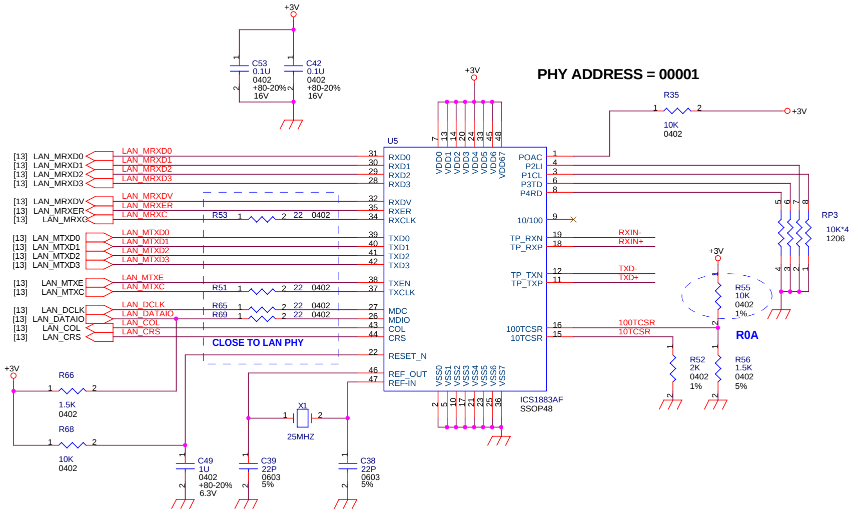
MiTAC

Title PCMCIA (Ti PCI1410A)

Size Document Number 411682900001 Rev R06

Date: Monday, April 12, 2004 Sheet 16 of 28

LAN PHY (ICS1883AF) & MDC


PHY ADDRESS = 00001
+3V
C53 0.1U 0402 +80-20% 16V
C42 0.1U 0402 +80-20% 16V
U5
ICS1883AF
SSOP48
[13] LAN_MRXD0
[13] LAN_MRXD1
[13] LAN_MRXD2
[13] LAN_MRXD3
[13] LAN_MRXDV
[13] LAN_MRXER
[13] LAN_MRXC
[13] LAN_MTXD0
[13] LAN_MTXD1
[13] LAN_MTXD2
[13] LAN_MTXD3
[13] LAN_MTXE
[13] LAN_MTXC
[13] LAN_DCLK
[13] LAN_DATAIO
[13] LAN_COL
[13] LAN_CRS
RXD0
RXD1
RXD2
RXD3
RXDV
RXER
RXCLK
TXD0
TXD1
TXD2
TXD3
TXEN
TXCLK
MDC
MDIO
COL
CRS
RESET_N
REF_OUT
REF-IN
POAC
P2LI
P1CL
P3TD
P4RD
10/100
TP_RXN
TP_RXP
TP_TXN
TP_TXP
100TCSR
10TCSR
RXIN-
RXIN+
TXD-
TXD+
R53 22 0402
R51 22 0402
R65 22 0402
R69 22 0402
CLOSE TO LAN PHY
R35 10K 0402
RP3 10K*4 1206
R55 10K 0402 1%
R0A
R52 2K 0402 1%
R56 1.5K 0402 5%
R66 1.5K 0402
R68 10K 0402
X1 25MHZ
C49 1U 0402 +80-20% 6.3V
C39 22P 0603 5%
C38 22P 0603 5%

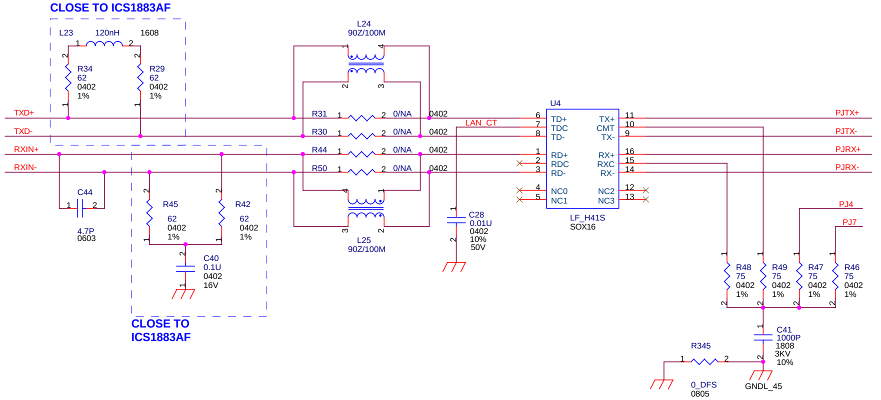
Layout Note:

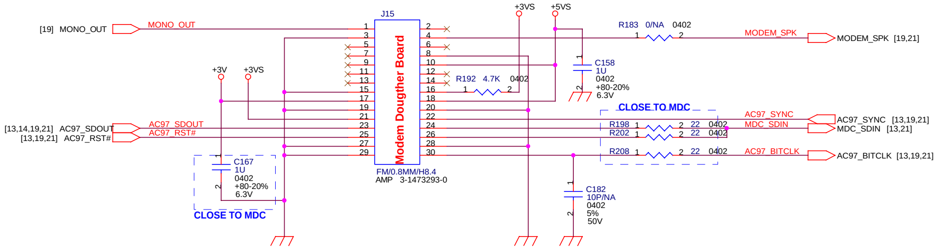
二組各自平行走線等長

二組中間須絕緣, EX: GND SHIELDING

S/W/W/S=10/8/8/10 mils

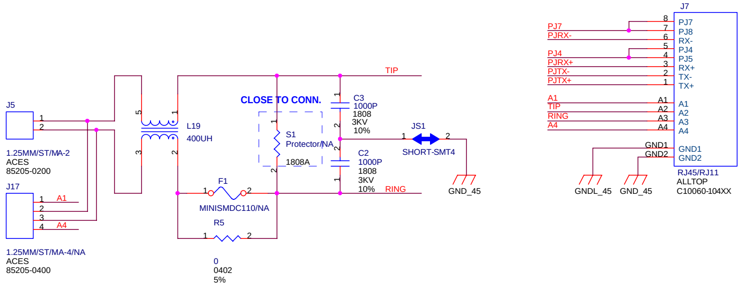
as short as possible


CLOSE TO ICS1883AF
L23 120nH 1608
R34 62 0402 1%
R29 62 0402 1%
TXD+
TXD-
RXIN+
RXIN-
C44 4.7P 0603
R45 62 0402 1%
R42 62 0402 1%
C40 0.1U 0402 16V
CLOSE TO ICS1883AF
L24 90Z/100M
L25 90Z/100M
R31 0/NA 0402
R30 0/NA 0402
R44 0/NA 0402
R50 0/NA 0402
LAN_CT
C28 0.01U 0402 10% 50V
U4
LF_H41S
SOX16
TD+
TDC
TD-
RD+
RDC
RD-
NC0
NC1
TX+
CMT
TX-
RX+
RXC
RX-
NC2
NC3
PJTX+
PJTX-
PJRX+
PJRX-
PJ4
PJ7
R48 75 0402 1%
R49 75 0402 1%
R47 75 0402 1%
R46 75 0402 1%
C41 1000P 1808 3KV 10%
R345 0_DFS 0805
GNDL_45


[19] MONO_OUT
MONO_OUT
J15
Modem Dougther Board
FM/0.8MM/H8.4
AMP 3-1473293-0
+3V
+3VS
+5VS
[13,14,19,21] AC97_SDOUT
[13,19,21] AC97_RST#
C167 1U 0402 +80-20% 6.3V
CLOSE TO MDC
R183 0/NA 0402
MODEM_SPK
MODEM_SPK [19,21]
C158 1U 0402 +80-20% 6.3V
R192 4.7K 0402
CLOSE TO MDC
R198 22 0402
R202 22 0402
R208 22 0402
AC97_SYNC
MDC_SDIN
AC97_BITCLK
AC97_SYNC [13,19,21]
MDC_SDIN [13,21]
AC97_BITCLK [13,19,21]
C182 10P/NA 0402 5% 50V

MDC HARDWARE STRAP

	HIGH	LOW
PIN 16	AUDIO CODEC ON MOTHER BD	AUDIO CODEC ON DAUGHTER BOARD


J5
1.25MM/ST/MA-2
ACES
85205-0200
J17
1.25MM/ST/MA-4/NA
ACES
85205-0400
A1
A4
L19 400UH
CLOSE TO CONN.
S1 Protector/NA 1808A
F1 MINISMDC110/NA
R5 0 0402 5%
C3 1000P 1808 3KV 10%
C2 1000P 1808 3KV 10%
TIP
RING
JS1 SHORT-SMT4
GND_45
J7
PJ7
PJ8
RX-
PJ4
PJ5
RX+
TX-
TX+
A1
A2
A3
A4
GND1
GND2
RJ45/RJ11
ALLTOP
C10060-104XX
PJRX-
PJRX+
PJTX-
PJTX+
TIP
RING
GNDL_45
GND_45

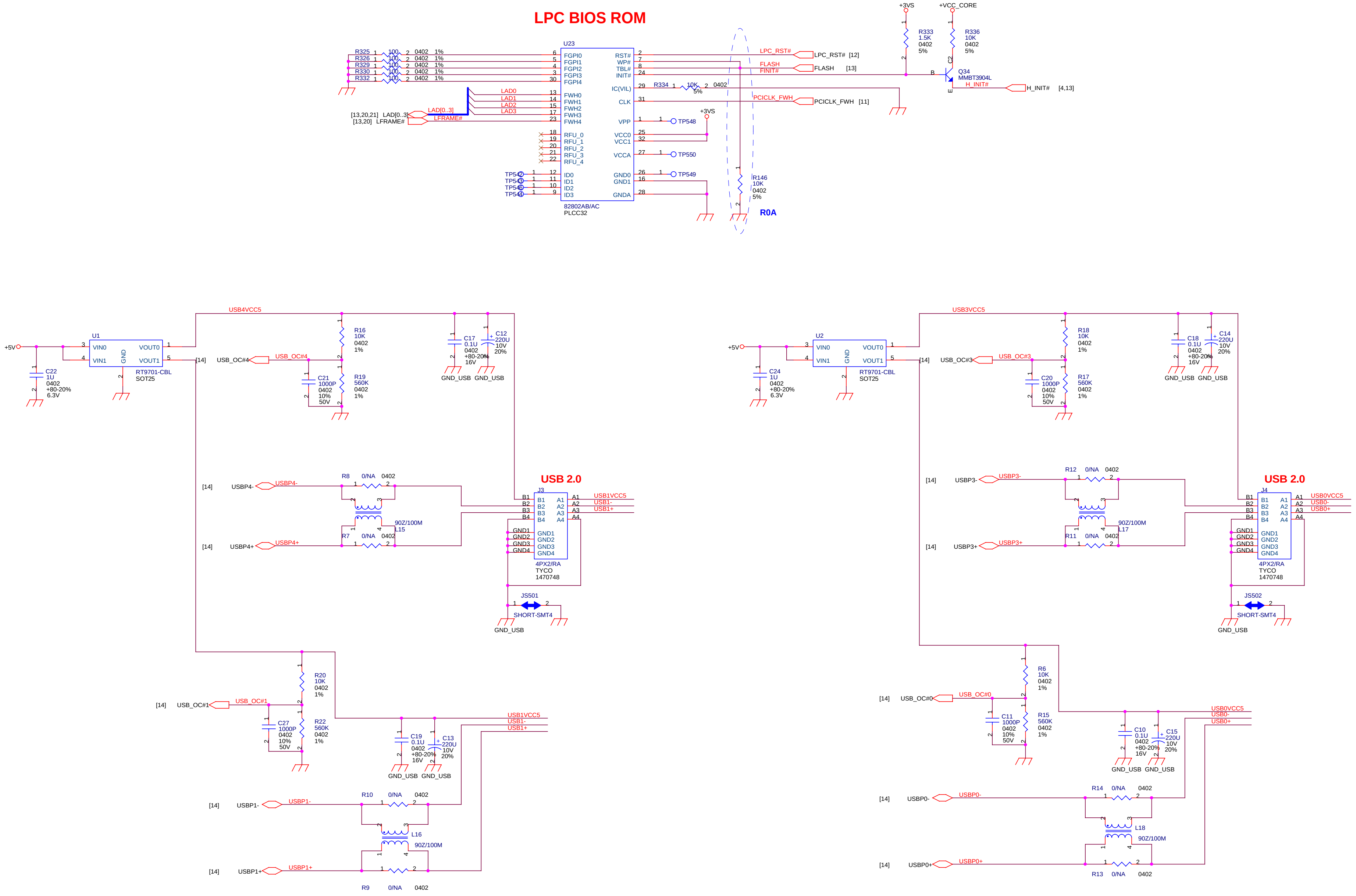
MiTAC

Title
LAN PHY (ICS1883AF) & MDC

Size
Document Number **411682900001**
Rev R06

Date: Monday, April 12, 2004
Sheet 17 of 28

USB 2.0 & Flash ROM


LPC BIOS ROM
U23
82802AB/AC
PLCC32
FGPI0
FGPI1
FGPI2
FGPI3
FGPI4
FWH0
FWH1
FWH2
FWH3
FWH4
RFU_0
RFU_1
RFU_2
RFU_3
RFU_4
ID0
ID1
ID2
ID3
RST#
WP#
TBL#
INIT#
IC(VIL)
CLK
VPP
VCC0
VCC1
VCCA
GND0
GND1
GNDA
R325
R326
R329
R330
R332
100
0402
1%
LAD0
LAD1
LAD2
LAD3
[13,20,21] LAD[0..3]
[13,20] LFRAME#
LAD[0..3]
LFRAME#
TP542
TP543
TP544
TP545
TP548
TP550
TP549
+3VS
R334 10K 5% 0402
LPC_RST#
LPC_RST# [12]
FLASH
FINIT#
FLASH [13]
PCICLK_FWH
PCICLK_FWH [11]
R146
10K
0402
5%
R0A
+3VS
+VCC_CORE
R333
1.5K
0402
5%
R336
10K
0402
5%
Q34
MMBT3904L
H_INIT#
H_INIT# [4,13]
USB4VCC5
U1
RT9701-CBL
SOT25
VIN0
VIN1
VOUT0
VOUT1
GND
+5V
C22
1U
0402
+80-20%
6.3V
[14] USB_OC#4
USB_OC#4
R16
10K
0402
1%
R19
560K
0402
1%
C21
1000P
0402
10%
50V
C17
0.1U
0402
+80-20%
16V
C12
220U
10V
20%
GND_USB
USB 2.0
J3
4PX2/RA
TYCO
1470748
B1
B2
B3
B4
A1
A2
A3
A4
GND1
GND2
GND3
GND4
USB1VCC5
USB1-
USB1+
[14] USBP4-
USBP4-
[14] USBP4+
USBP4+
R8 0/NA 0402
R7 0/NA 0402
L15
90Z/100M
JS501
SHORT-SMT4
GND_USB
USB3VCC5
U2
RT9701-CBL
SOT25
C24
1U
0402
+80-20%
6.3V
[14] USB_OC#3
USB_OC#3
R18
10K
0402
1%
R17
560K
0402
1%
C20
1000P
0402
10%
50V
C18
0.1U
0402
+80-20%
16V
C14
220U
10V
20%
USB 2.0
J4
4PX2/RA
TYCO
1470748
USB0VCC5
USB0-
USB0+
[14] USBP3-
USBP3-
[14] USBP3+
USBP3+
R12 0/NA 0402
R11 0/NA 0402
L17
90Z/100M
JS502
SHORT-SMT4
[14] USB_OC#1
USB_OC#1
R20
10K
0402
1%
R22
560K
0402
1%
C27
1000P
0402
10%
50V
C19
0.1U
0402
+80-20%
16V
C13
220U
10V
20%
USB1VCC5
USB1-
USB1+
[14] USBP1-
USBP1-
[14] USBP1+
USBP1+
R10 0/NA 0402
R9 0/NA 0402
L16
90Z/100M
[14] USB_OC#0
USB_OC#0
R6
10K
0402
1%
R15
560K
0402
1%
C11
1000P
0402
10%
50V
C10
0.1U
0402
+80-20%
16V
C15
220U
10V
20%
USB0VCC5
USB0-
USB0+
[14] USBP0-
USBP0-
[14] USBP0+
USBP0+
R14 0/NA 0402
R13 0/NA 0402
L18
90Z/100M

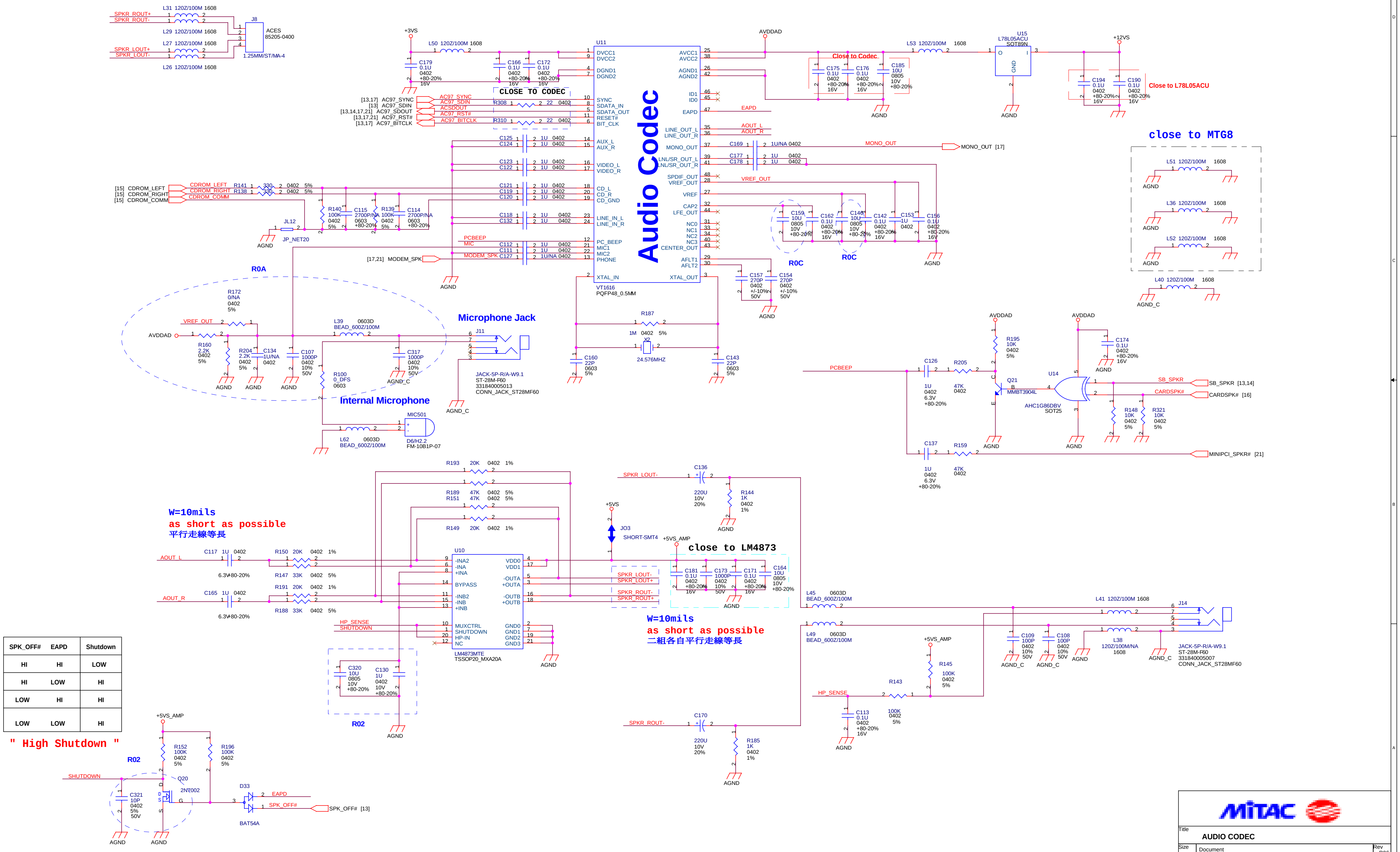
MiTAC

Title
USB 2.0 & Flash ROM

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 18 of 28

AUDIO CODEC



SPKR_ROUT+
SPKR_ROUT-
SPKR_LOUT+
SPKR_LOUT-
L31 120Z/100M 1608
L29 120Z/100M 1608
L27 120Z/100M 1608
L26 120Z/100M 1608
J8
ACES
85205-0400
1.25MM/ST/MA-4
+3VS
L50 120Z/100M 1608
C179 0.1U 0402 +80-20% 16V
C166 0.1U 0402 +80-20% 16V
C172 0.1U 0402 +80-20% 16V
CLOSE TO CODEC
[13,17] AC97_SYNC
[13] AC97_SDIN
[13,14,17,21] AC97_SDOUT
[13,17,21] AC97_RST#
[13,17] AC97_BITCLK
AC97_SYNC
AC97_SDIN
ACSDOUT
AC97_RST#
AC97_BITCLK
R308 22 0402
R310 22 0402
U11
Audio Codec
DVCC1
DVCC2
DGND1
DGND2
SYNC
SDATA_IN
SDATA_OUT
RESET#
BIT_CLK
AUX_L
AUX_R
VIDEO_L
VIDEO_R
CD_L
CD_R
CD_GND
LINE_IN_L
LINE_IN_R
PC_BEEP
MIC1
MIC2
PHONE
XTAL_IN
XTAL_OUT
AVCC1
AVCC2
AGND1
AGND2
ID1
ID0
EAPD
LINE_OUT_L
LINE_OUT_R
MONO_OUT
LNL/SR_OUT_L
LNL/SR_OUT_R
SPDIF_OUT
VREF_OUT
VREF
CAP2
LFE_OUT
NC0
NC1
NC2
NC3
CENTER_OUT
AFLT1
AFLT2
VT1616
PQFP48_0.5MM
C125 1U 0402
C124 1U 0402
C123 1U 0402
C122 1U 0402
C121 1U 0402
C119 1U 0402
C120 1U 0402
C118 1U 0402
C132 1U 0402
C112 1U 0402
C111 1U 0402
C127 1U/NA 0402
[15] CDROM_LEFT
[15] CDROM_RIGHT
[15] CDROM_COMM
CDROM_LEFT
CDROM_RIGHT
CDROM_COMM
R141 330 0402 5%
R138 330 0402 5%
R140 100K 0402 5%
C115 2700P/NA 0603 +80-20%
R139 100K 0402 5%
C114 2700P/NA 0603 +80-20%
JL12
JP_NET20
PCBEEP
MIC
MODEM_SPK
[17,21] MODEM_SPK
AGND
AVDDAD
EAPD
AOUT_L
AOUT_R
C169 1U/NA 0402
MONO_OUT
MONO_OUT [17]
C177 1U 0402
C178 1U 0402
VREF_OUT
L53 120Z/100M 1608
U15
L78L05ACU
SOT89N
O
I
GND
Close to Codec
C175 0.1U 0402 +80-20% 16V
C176 0.1U 0402 +80-20% 16V
C185 10U 0805 10V +80-20%
+12VS
C194 0.1U 0402 +80-20% 16V
C190 0.1U 0402 +80-20% 16V
Close to L78L05ACU
C159 10U 0805 10V +80-20%
C162 0.1U 0402 +80-20% 16V
C140 10U 0805 10V +80-20%
C142 0.1U 0402 +80-20% 16V
C153 1U 0402
C156 0.1U 0402 +80-20% 16V
R0C
R0C
C157 270P 0402 +/-10% 50V
C154 270P 0402 +/-10% 50V
close to MTG8
L51 120Z/100M 1608
L36 120Z/100M 1608
L52 120Z/100M 1608
L40 120Z/100M 1608
AGND_C
R0A
R172 0/NA 0402 5%
VREF_OUT
R160 2.2K 0402 5%
R204 2.2K 0402 5%
C134 1U/NA 0402
C107 1000P 0402 10% 50V
L39 0603D BEAD_600Z/100M
C317 1000P 0402 10% 50V
R100 0_DFS 0603
Microphone Jack
J11
JACK-5P-R/A-W9.1
ST-28M-F60
331840005013
CONN_JACK_ST28MF60
Internal Microphone
MIC501
D6/H2.2
FM-10B1P-07
L62 0603D BEAD_600Z/100M
R187 1M 0402 5%
X2 24.576MHZ
C160 22P 0603 5%
C143 22P 0603 5%
AVDDAD
R195 10K 0402 5%
C174 0.1U 0402 +80-20% 16V
PCBEEP
C126 1U 0402 6.3V +80-20%
R205 47K 0402
Q21 MMBT3904L
U14 AHC1G86DBV SOT25
SB_SPKR
SB_SPKR [13,14]
CARDSPK#
CARDSPK# [16]
R148 10K 0402 5%
R321 10K 0402 5%
C137 1U 0402 6.3V +80-20%
R159 47K 0402
MINIPCI_SPKR# [21]
R193 20K 0402 1%
R189 47K 0402 5%
R151 47K 0402 5%
R149 20K 0402 1%
SPKR_LOUT-
C136 220U 10V 20%
R144 1K 0402 1%
+5VS
JO3 SHORT-SMT4
+5VS_AMP
close to LM4873
W=10mils
as short as possible
平行走線等長
AOUT_L
C117 1U 0402 6.3V +80-20%
AOUT_R
C165 1U 0402 6.3V +80-20%
R150 20K 0402 1%
R147 33K 0402 5%
R191 20K 0402 1%
R188 33K 0402 5%
U10
-INA2
-INA
+INA
BYPASS
-INB2
-INB
+INB
MUXCTRL
SHUTDOWN
HP-IN
NC
VDD0
VDD1
-OUTA
+OUTA
-OUTB
+OUTB
GND0
GND1
GND2
GND3
LM4873MTE
TSSOP20_MXA20A
HP_SENSE
SHUTDOWN
C320 10U 0805 10V +80-20%
C130 1U 0402 10V +80-20%
R02
SPKR_LOUT-
SPKR_LOUT+
SPKR_ROUT-
SPKR_ROUT+
C181 0.1U 0402 +80-20% 16V
C173 1000P 0402 10% 50V
C171 0.1U 0402 +80-20% 16V
C164 10U 0805 10V +80-20%
W=10mils
as short as possible
二組各自平行走線等長
L45 0603D BEAD_600Z/100M
L49 0603D BEAD_600Z/100M
L41 120Z/100M 1608
J14
C109 100P 0402 10% 50V
C108 100P 0402 10% 50V
L38 120Z/100M/NA 1608
JACK-5P-R/A-W9.1
ST-28M-F60
331840005007
CONN_JACK_ST28MF60
+5VS_AMP
R145 100K 0402 5%
R143 100K 0402 5%
HP_SENSE
C113 0.1U 0402 +80-20% 16V
SPKR_ROUT-
C170 220U 10V 20%
R185 1K 0402 1%
+5VS_AMP
R152 100K 0402 5%
R196 100K 0402 5%
R02
SHUTDOWN
C321 10P 0402 5% 50V
Q20 2N7002
D33 BAT54A
EAPD
SPK_OFF#
SPK_OFF# [13]

SPK_OFF#	EAPD	Shutdown
HI	HI	LOW
HI	LOW	HI
LOW	HI	HI
LOW	LOW	HI

" High Shutdown "

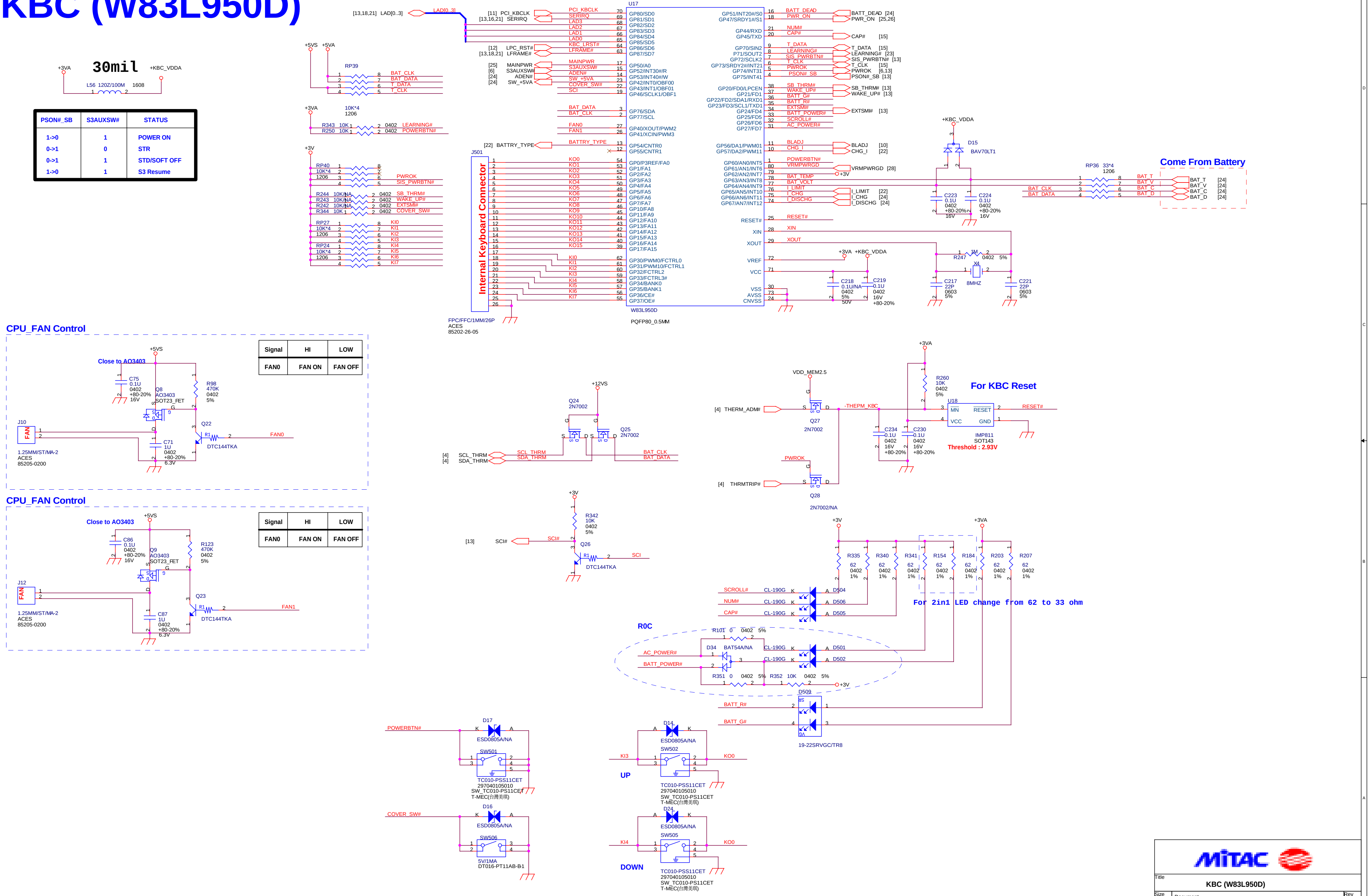
MiTAC

Title AUDIO CODEC

Size Document Number 411682900001 Rev R06

Date: Monday, April 12, 2004 Sheet 19 of 28

KBC (W83L950D)


30mil
+3VA
+KBC_VDDA
L56 120Z/100M 1608
+5VS +5VA
RP39
BAT_CLK
BAT_DATA
T_DATA
T_CLK
+3VA 10K*4 1206
R343 10K 0402 LEARNING#
R250 10K 0402 POWERBTN#
+3V
RP40 10K*4 1206
PWROK
SIS_PWRBTN#
R244 10K/NA 0402 SB_THRM#
R243 10K/NA 0402 WAKE_UP#
R242 10K/NA 0402 EXTSMI#
R344 10K 0402 COVER_SW#
RP27 10K*4 1206
RP24 10K*4 1206
KI0 KI1 KI2 KI3 KI4 KI5 KI6 KI7
[13,18,21] LAD[0..3]
LAD[0..3]
[11] PCI_KBCLK
[13,16,21] SERIRQ
[12] LPC_RST#
[13,18,21] LFRAME#
[25] MAINPWR
[6] S3AUXSW#
[24] ADEN#
[24] SW_+5VA
[22] BATTRY_TYPE
J501
Internal Keyboard Connector
FPC/FFC/1MM/26P
ACES
85202-26-05
KO0 KO1 KO2 KO3 KO4 KO5 KO6 KO7 KO8 KO9 KO10 KO11 KO12 KO13 KO14 KO15
U17
GP80/SD0
GP81/SD1
GP82/SD2
GP83/SD3
GP84/SD4
GP85/SD5
GP86/SD6
GP87/SD7
GP50/A0
GP52/INT30#/R
GP53/INT40#/W
GP42/INT0/OBF00
GP43/INT1/OBF01
GP46/SCLK1/OBF1
GP76/SDA
GP77/SCL
GP40/XOUT/PWM2
GP41/XCIN/PWM3
GP54/CNTR0
GP55/CNTR1
GP0/P3REF/FA0
GP1/FA1 … GP17/FA15
GP30/PWM0/FCTRL0
GP31/PWM10/FCTRL1
GP32/FCTRL2
GP33/FCTRL3#
GP34/BANK0
GP35/BANK1
GP36/CE#
GP37/OE#
GP51/INT20#/S0
GP47/SRDY1#/S1
GP44/RXD
GP45/TXD
GP70/SIN2
P71/SOUT2
GP72/SCLK2
GP73/SRDY2#/INT21
GP74/INT31
GP75/INT41
GP20/FD0/LPCEN
GP21/FD1
GP22/FD2/SDA1/RXD1
GP23/FD3/SCL1/TXD1
GP24/FD4
GP25/FD5
GP26/FD6
GP27/FD7
GP56/DA1/PWM01
GP57/DA2/PWM11
GP60/AN0/INT5
GP61/AN1/INT6
GP62/AN2/INT7
GP63/AN3/INT8
GP64/AN4/INT9
GP65/AN5/INT10
GP66/AN6/INT11
GP67/AN7/INT12
RESET#
XIN
XOUT
VREF
VCC
VSS
AVSS
CNVSS
W83L950D
PQFP80_0.5MM
BATT_DEAD [24]
PWR_ON [25,26]
NUM#
CAP# [15]
T_DATA [15]
LEARNING# [23]
SIS_PWRBTN# [13]
T_CLK [15]
PWROK [6,13]
PSON#_SB [13]
SB_THRM# [13]
WAKE_UP# [13]
BATT_G#
BATT_R#
EXTSMI# [13]
BATT_POWER#
SCROLL#
AC_POWER#
BLADJ [10]
CHG_I [22]
POWERBTN#
VRMPWRGD [28]
BAT_TEMP
BAT_VOLT
I_LIMIT [22]
I_CHG [24]
I_DISCHG [24]
+KBC_VDDA
D15 BAV70LT1
RP36 33*4 1206
Come From Battery
BAT_T [24]
BAT_V [24]
BAT_C [24]
BAT_D [24]
C223 0.1U 0402 +80-20% 16V
C224 0.1U 0402 +80-20% 16V
R247 1M 0402 5%
X4 8MHZ
C217 22P 0603 5%
C221 22P 0603 5%
C218 0.1U/NA 0402 5% 50V
C219 0.1U 0402 16V +80-20%
CPU_FAN Control
Close to AO3403
C75 0.1U 0402 +80-20% 16V
Q8 AO3403 SOT23_FET
R98 470K 0402 5%
J10
FAN
1.25MM/ST/MA-2
ACES
85205-0200
C71 1U 0402 +80-20% 6.3V
Q22 DTC144TKA
FAN0
+12VS
Q24 2N7002
Q25 2N7002
[4] SCL_THRM
[4] SDA_THRM
BAT_CLK
BAT_DATA
CPU_FAN Control
Close to AO3403
C86 0.1U 0402 +80-20% 16V
Q9 AO3403 SOT23_FET
R123 470K 0402 5%
J12
C87 1U 0402 +80-20% 6.3V
Q23 DTC144TKA
FAN1
+3V
R342 10K 0402 5%
[13] SCI#
Q26 DTC144TKA
SCI
VDD_MEM2.5
[4] THERM_ADM#
Q27 2N7002
-THEPM_KBC
+3VA
R260 10K 0402 5%
For KBC Reset
U18
MN RESET
VCC GND
C234 0.1U 0402 16V +80-20%
C230 0.1U 0402 16V +80-20%
IMP811 SOT143
Threshold : 2.93V
RESET#
PWROK
[4] THRMTRIP#
Q28 2N7002/NA
R335 62 0402 1%
R340 62 0402 1%
R341 62 0402 1%
R154 62 0402 1%
R184 62 0402 1%
R203 62 0402 1%
R207 62 0402 1%
CL-190G
D504 D506 D505
For 2in1 LED change from 62 to 33 ohm
R0C
R101 0 0402 5%
D34 BAT54A/NA
D501 D502
R351 0 0402 5%
R352 10K 0402 5%
D509
BATT_R#
BATT_G#
19-22SRVGC/TR8
POWERBTN#
D17 ESD0805A/NA
SW501
TC010-PSS11CET
297040105010
SW_TC010-PSS11CET
T-MEC(台灣美琪)
COVER_SW#
D16 ESD0805A/NA
SW506
5V/1MA
DT016-PT11AB-B1
KI3
D14 ESD0805A/NA
SW502
KO0
UP
KI4
D24 ESD0805A/NA
SW505
DOWN

PSON#_SB	S3AUXSW#	STATUS
1->0	1	POWER ON
0->1	0	STR
0->1	1	STD/SOFT OFF
1->0	1	S3 Resume

Signal	HI	LOW
FAN0	FAN ON	FAN OFF

Signal	HI	LOW
FAN0	FAN ON	FAN OFF

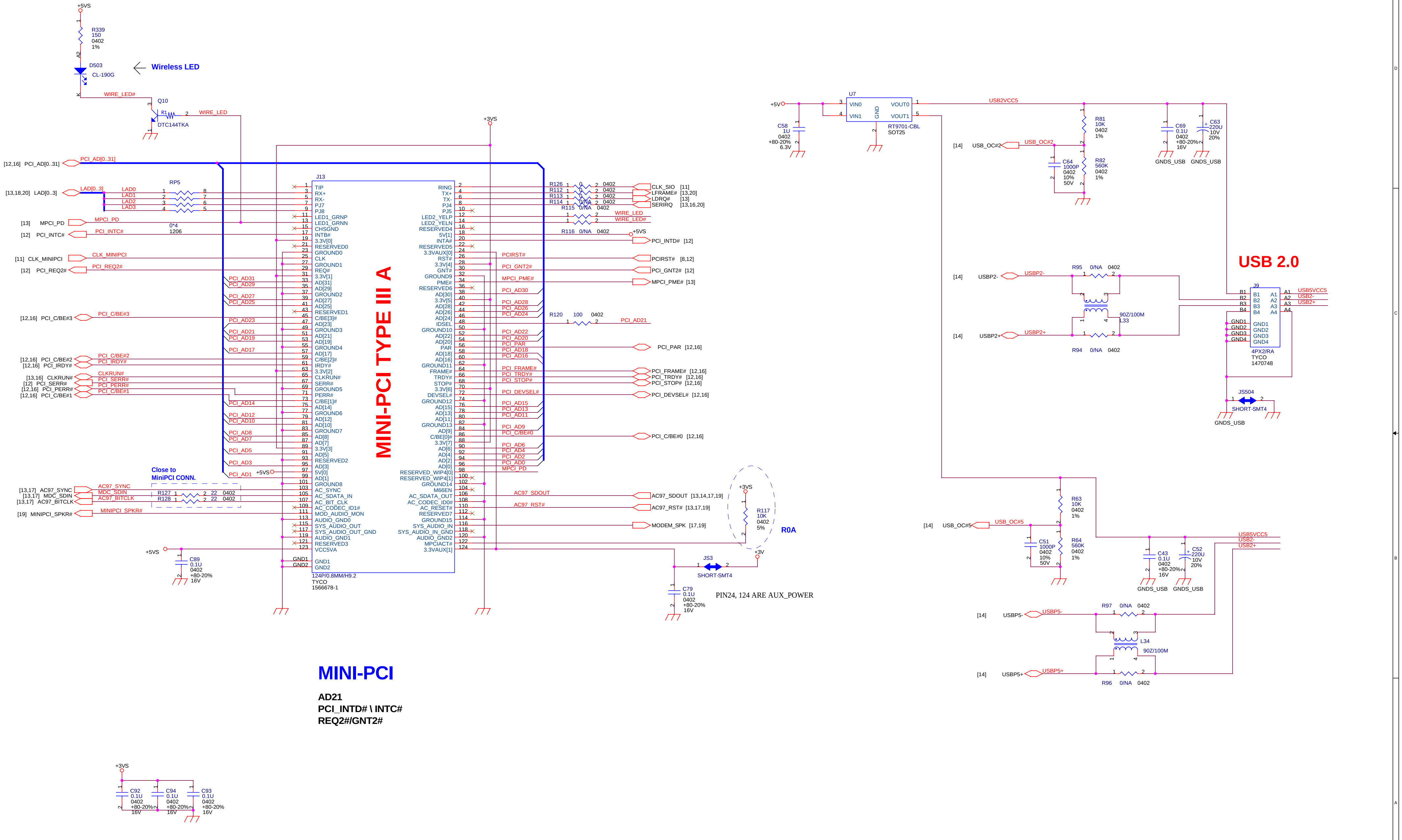
MiTAC

Title
KBC (W83L950D)

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 20 of 28

Mini-PCI & USB 2.0

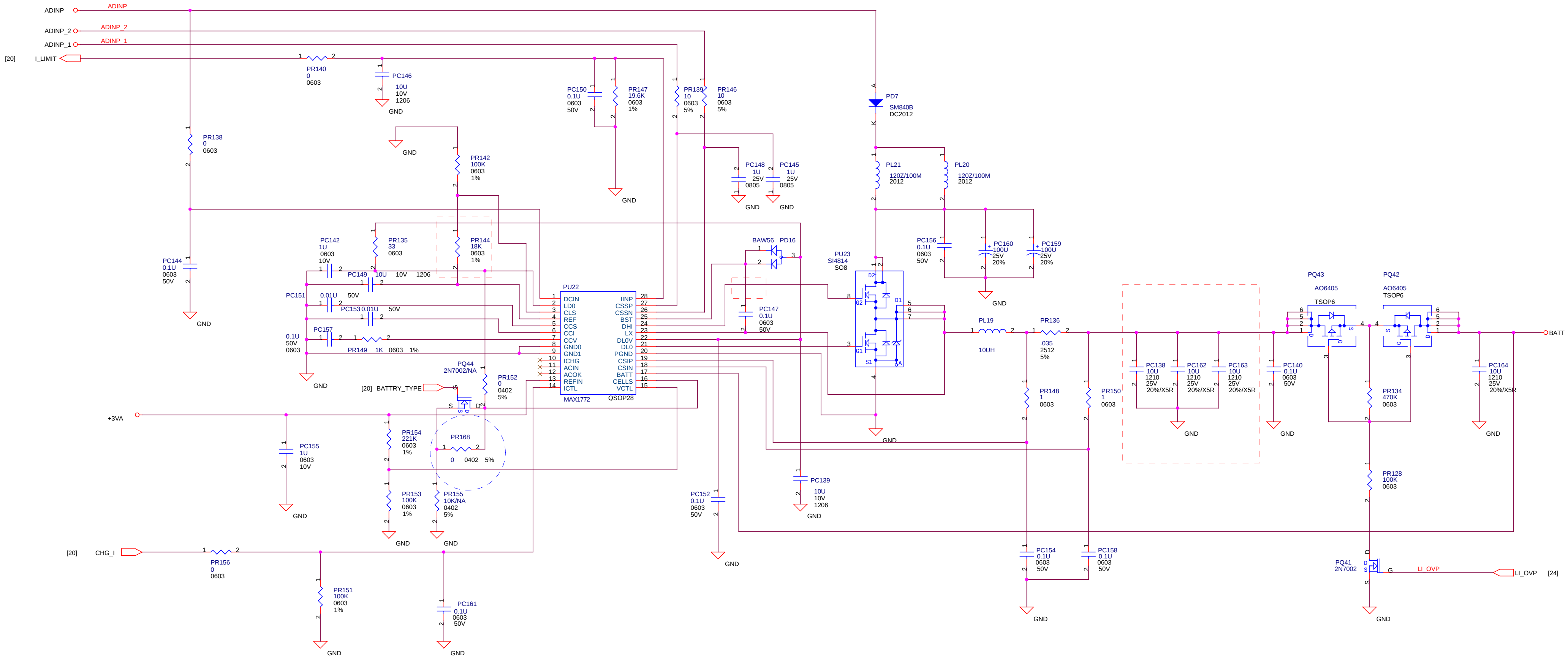

+5VS
R339
150
0402
1%
D503
CL-190G
Wireless LED
WIRE_LED#
Q10
DTC144TKA
WIRE_LED
+3VS
[12,16] PCI_AD[0..31]
PCI_AD[0..31]
[13,18,20] LAD[0..3]
LAD[0..3]
LAD0
LAD1
LAD2
LAD3
RP5
0*4
1206
[13] MPCI_PD
MPCI_PD
[12] PCI_INTC#
PCI_INTC#
[11] CLK_MINIPCI
CLK_MINIPCI
[12] PCI_REQ2#
PCI_REQ2#
[12,16] PCI_C/BE#3
PCI_C/BE#3
[12,16] PCI_C/BE#2
[12,16] PCI_IRDY#
[13,16] CLKRUN#
[12] PCI_SERR#
[12,16] PCI_PERR#
[12,16] PCI_C/BE#1
Close to
MiniPCI CONN.
[13,17] AC97_SYNC
[13,17] MDC_SDIN
[13,17] AC97_BITCLK
[19] MINIPCI_SPKR#
R127 22 0402
R128 22 0402
+5VS
C89
0.1U
0402
+80-20%
16V
J13
124P/0.8MM/H9.2
TYCO
1566678-1
MINI-PCI TYPE III A
R126 0 0402
R112 0 0402
R113 0 0402
R114 0/NA 0402
R115 0/NA 0402
R116 0/NA 0402
CLK_SIO [11]
LFRAME# [13,20]
LDRQ# [13]
SERIRQ [13,16,20]
WIRE_LED
WIRE_LED#
+5VS
PCI_INTD# [12]
PCIRST# [8,12]
PCI_GNT2# [12]
MPCI_PME# [13]
R120 100 0402
PCI_AD21
PCI_PAR [12,16]
PCI_FRAME# [12,16]
PCI_TRDY# [12,16]
PCI_STOP# [12,16]
PCI_DEVSEL# [12,16]
PCI_C/BE#0 [12,16]
AC97_SDOUT [13,14,17,19]
AC97_RST# [13,17,19]
MODEM_SPK [17,19]
+3VS
R117
10K
0402
5%
R0A
JS3
SHORT-SMT4
+3V
C79
0.1U
0402
+80-20%
16V
PIN24, 124 ARE AUX_POWER
U7
RT9701-CBL
SOT25
+5V
C58
1U
0402
+80-20%
6.3V
USB2VCC5
R81
10K
0402
1%
R82
560K
0402
1%
C64
1000P
0402
10%
50V
[14] USB_OC#2
C69
0.1U
0402
+80-20%
16V
C63
220U
10V
20%
GNDS_USB
USB 2.0
[14] USBP2-
[14] USBP2+
R95 0/NA 0402
R94 0/NA 0402
L33
90Z/100M
J9
4PX2/RA
TYCO
1470748
USB5VCC5
USB2-
USB2+
JS504
SHORT-SMT4
GNDS_USB
R63
10K
0402
1%
R64
560K
0402
1%
C51
1000P
0402
10%
50V
[14] USB_OC#5
C43
0.1U
0402
+80-20%
16V
C52
220U
10V
20%
USB5VCC5
USB2-
USB2+
[14] USBP5-
[14] USBP5+
R97 0/NA 0402
R96 0/NA 0402
L34
90Z/100M
MINI-PCI
AD21
PCI_INTD# \ INTC#
REQ2#/GNT2#
+3VS
C92 0.1U 0402 +80-20% 16V
C94 0.1U 0402 +80-20% 16V
C93 0.1U 0402 +80-20% 16V

MiTAC

Title
Mini-PCI & USB 2.0

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 21 of 28

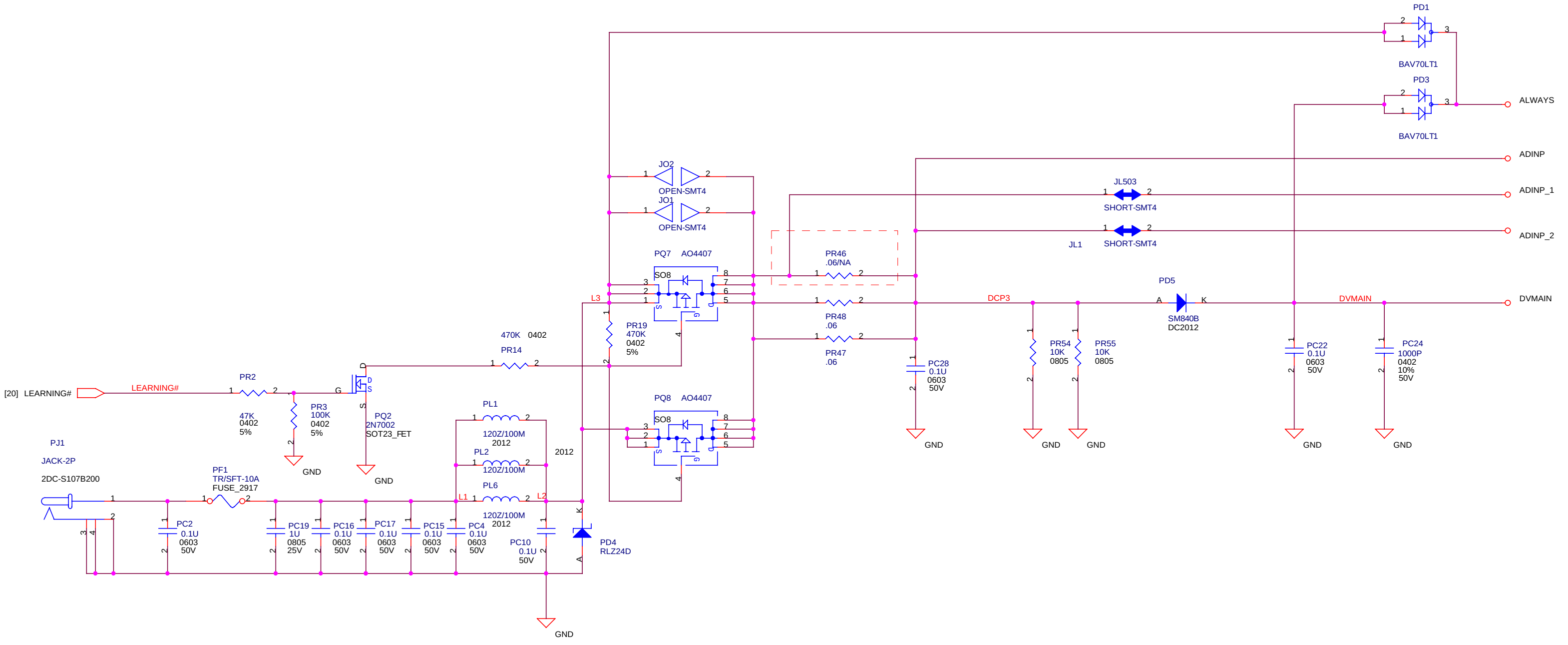

ADINP
ADINP
ADINP_2
ADINP_2
ADINP_1
ADINP_1
[20]
I_LIMIT
PR140
0
0603
PC146
10U
10V
1206
GND
PR138
0
0603
PC144
0.1U
0603
50V
GND
PR142
100K
0603
1%
GND
PC150
0.1U
0603
50V
PR147
19.6K
0603
1%
GND
PR139
10
0603
5%
PR146
10
0603
5%
PC148
1U
25V
0805
PC145
1U
25V
0805
GND
GND
PD7
SM840B
DC2012
PL21
120Z/100M
2012
PL20
120Z/100M
2012
PC156
0.1U
0603
50V
PC160
100U
25V
20%
PC159
100U
25V
20%
GND
PC142
1U
0603
10V
PR135
33
0603
PR144
18K
0603
1%
PC149
10U
10V
1206
PC151
0.01U
50V
PC153
0.01U
50V
PC157
0.1U
50V
0603
PR149
1K
0603
1%
GND
PU22
DCIN
LDO
CLS
REF
CCS
CCI
CCV
GND0
GND1
ICHG
ACIN
ACOK
REFIN
ICTL
IINP
CSSP
CSSN
BST
DHI
LX
DLOV
DLO
PGND
CSIP
CSIN
BATT
CELLS
VCTL
MAX1772
QSOP28
BAW56
PD16
PC147
0.1U
0603
50V
PU23
SI4814
SO8
D2
G2
D1
G1
S1
S/A
PL19
10UH
PR136
.035
2512
5%
PC138
10U
1210
25V
20%/X5R
PC162
10U
1210
25V
20%/X5R
PC163
10U
1210
25V
20%/X5R
GND
PC140
0.1U
0603
50V
GND
PQ43
AO6405
TSOP6
PQ42
AO6405
TSOP6
PC164
10U
1210
25V
20%/X5R
GND
BATT
PR134
470K
0603
PR128
100K
0603
PQ41
2N7002
LI_OVP
LI_OVP
[24]
GND
PR148
1
0603
PR150
1
0603
PC154
0.1U
0603
50V
PC158
0.1U
0603
50V
GND
PQ44
2N7002/NA
[20]
BATTERY_TYPE
PR152
0
0402
5%
+3VA
PC155
1U
0603
10V
GND
PR154
221K
0603
1%
PR168
0
0402
5%
PR153
100K
0603
1%
PR155
10K/NA
0402
5%
GND
GND
PC152
0.1U
0603
50V
GND
PC139
10U
10V
1206
GND
[20]
CHG_I
PR156
0
0603
PR151
100K
0603
1%
GND
PC161
0.1U
0603
50V
GND

MiTAC

Title
DC-DC CONNECTOR ,CHARGER

Size
Document Number 411682900001
Rev R06

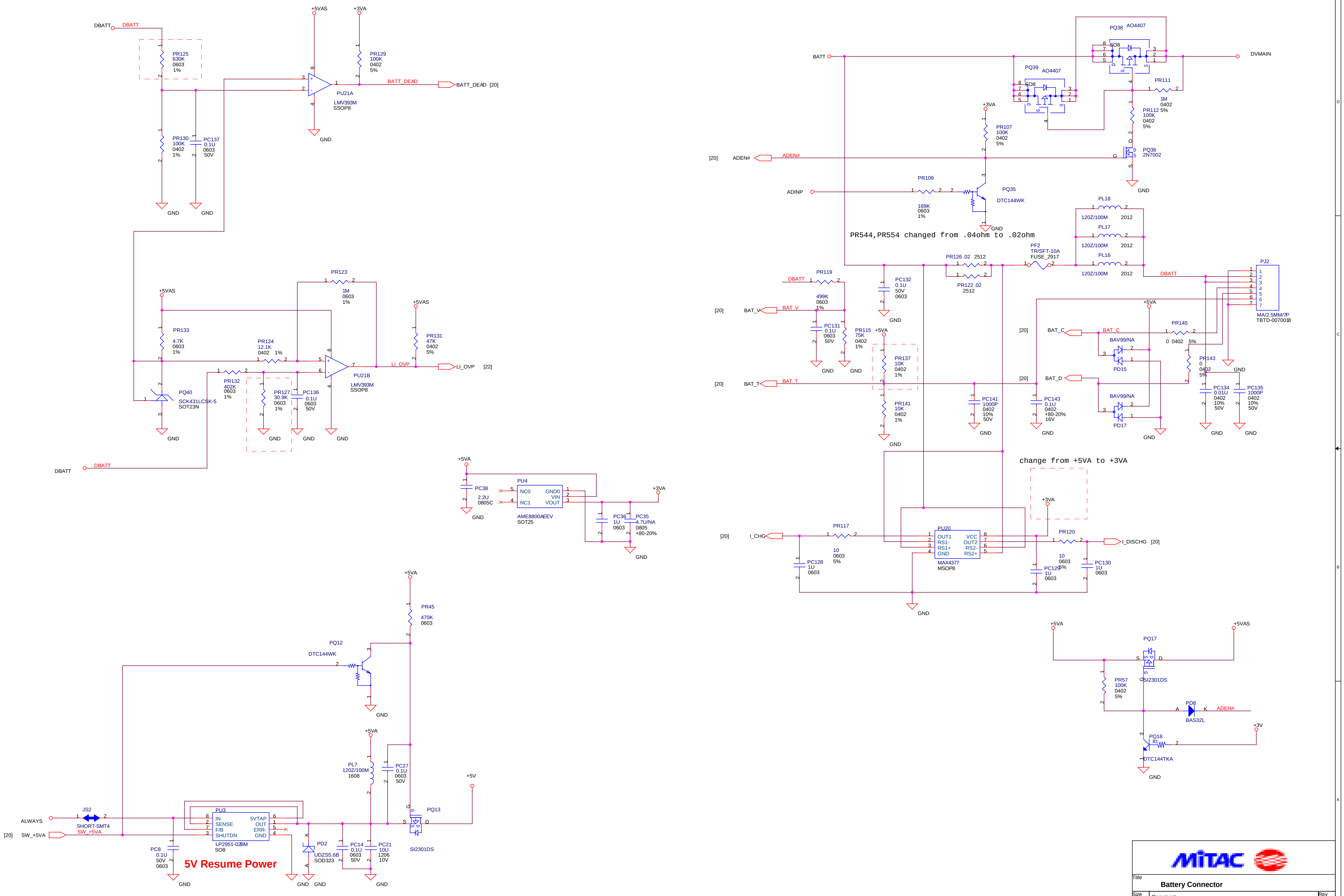
Date: Monday, April 12, 2004
Sheet 22 of 28


PD1
BAV70LT1
PD3
BAV70LT1
ALWAYS
ADINP
ADINP_1
ADINP_2
DVMAIN
JO2
OPEN-SMT4
JO1
OPEN-SMT4
JL503
SHORT-SMT4
JL1
SHORT-SMT4
PQ7 AO4407
SO8
PQ8 AO4407
SO8
PR46
.06/NA
PR48
.06
PR47
.06
L3
DCP3
PD5
A
K
SM840B
DC2012
DVMAIN
PR19
470K
0402
5%
470K 0402
PR14
PC28
0.1U
0603
50V
PR54
10K
0805
PR55
10K
0805
PC22
0.1U
0603
50V
PC24
1000P
0402
10%
50V
[20] LEARNING#
LEARNING#
PR2
47K
0402
5%
PR3
100K
0402
5%
G
D
S
PQ2
2N7002
SOT23_FET
PJ1
JACK-2P
2DC-S107B200
PF1
TR/SFT-10A
FUSE_2917
PL1
120Z/100M
2012
PL2
120Z/100M
PL6
120Z/100M
2012
2012
L1
L2
PC2
0.1U
0603
50V
PC19
1U
0805
25V
PC16
0.1U
0603
50V
PC17
0.1U
0603
50V
PC15
0.1U
0603
50V
PC4
0.1U
0603
50V
PC10
0.1U
50V
PD4
RLZ24D
GND

Title
DC Connector

Size
Document Number 411682900001
Rev R06

Date: Monday, April 12, 2004
Sheet 23 of 28


DBATT
PR125 630K 0603 1%
+5VAS
+3VA
PR129 100K 0402 5%
PU21A LMV393M SSOP8
BATT_DEAD
BATT_DEAD [20]
GND
PR130 100K 0402 1%
PC137 0.1U 0603 50V
PR123 1M 0603 1%
PR133 4.7K 0603 1%
PR124 12.1K 0402 1%
PR131 47K 0402 5%
PU21B LMV393M SSOP8
LI_OVP
LI_OVP [22]
PR132 402K 0603 1%
PQ40 SCK431LCSK-5 SOT23N
PR127 30.9K 0603 1%
PC136 0.1U 0603 50V
DBATT
+5VA
PC38 2.2U 0805C
PU4 NC0 NC1 GND0 VIN VOUT AME8800AEEV SOT25
PC36 1U 0603
PC35 4.7U/NA 0805 +80-20%
PR45 470K 0603
PQ12 DTC144WK
PL7 120Z/100M 1608
PC27 0.1U 0603 50V
PQ13 SI2301DS
+5V
ALWAYS
JS2 SHORT-SMT4
[20] SW_+5VA
SW_+5VA
PC8 0.1U 50V 0603
PU3 IN SENSE SHUTDN 5VTAP OUT ERR- GND LP2951-02BM SO8
PD2 UDZS5.6B SOD323
PC14 0.1U 0603 50V
PC21 10U 1206 10V
BATT
PQ38 AO4407 SO8
PQ39 AO4407 SO8
DVMAIN
PR111 1M 0402 5%
PR112 100K 0402 5%
PR107 100K 0402 5%
[20] ADEN#
ADEN#
PQ36 2N7002
ADINP
PR109 169K 0603 1%
PQ35 DTC144WK
PL18 120Z/100M 2012
PL17 120Z/100M 2012
PL16 120Z/100M 2012
PF2 TR/SFT-10A FUSE_2917
PR126 .02 2512
PR122 .02 2512
PR119 499K 0603 1%
PC132 0.1U 50V 0603
PJ2 MA/2.5MM/7P TBTD-0070018
[20] BAT_V
BAT_V
PC131 0.1U 0603 50V
PR115 75K 0402 1%
PR137 10K 0402 1%
[20] BAT_C
BAT_C
PR145 0 0402 5%
BAV99/NA PD15
PR143 0 0402 5%
[20] BAT_T
BAT_T
[20] BAT_D
PR141 10K 0402 1%
PC141 1000P 0402 10% 50V
PC143 0.1U 0402 +80-20% 16V
BAV99/NA PD17
PC134 0.01U 0402 10% 50V
PC135 1000P 0402 10% 50V
[20] I_CHG
PR117 10 0603 5%
PC128 1U 0603
PU20 OUT1 RS1- RS1+ GND VCC OUT2 RS2- RS2+ MAX4377 MSOP8
PR120 10 0603 5%
PC129 1U 0603
PC130 1U 0603
I_DISCHG [20]
PQ17 SI2301DS
PR57 100K 0402 5%
PD8 BAS32L
+3V
PQ18 DTC144TKA

PR544,PR554 changed from .04ohm to .02ohm

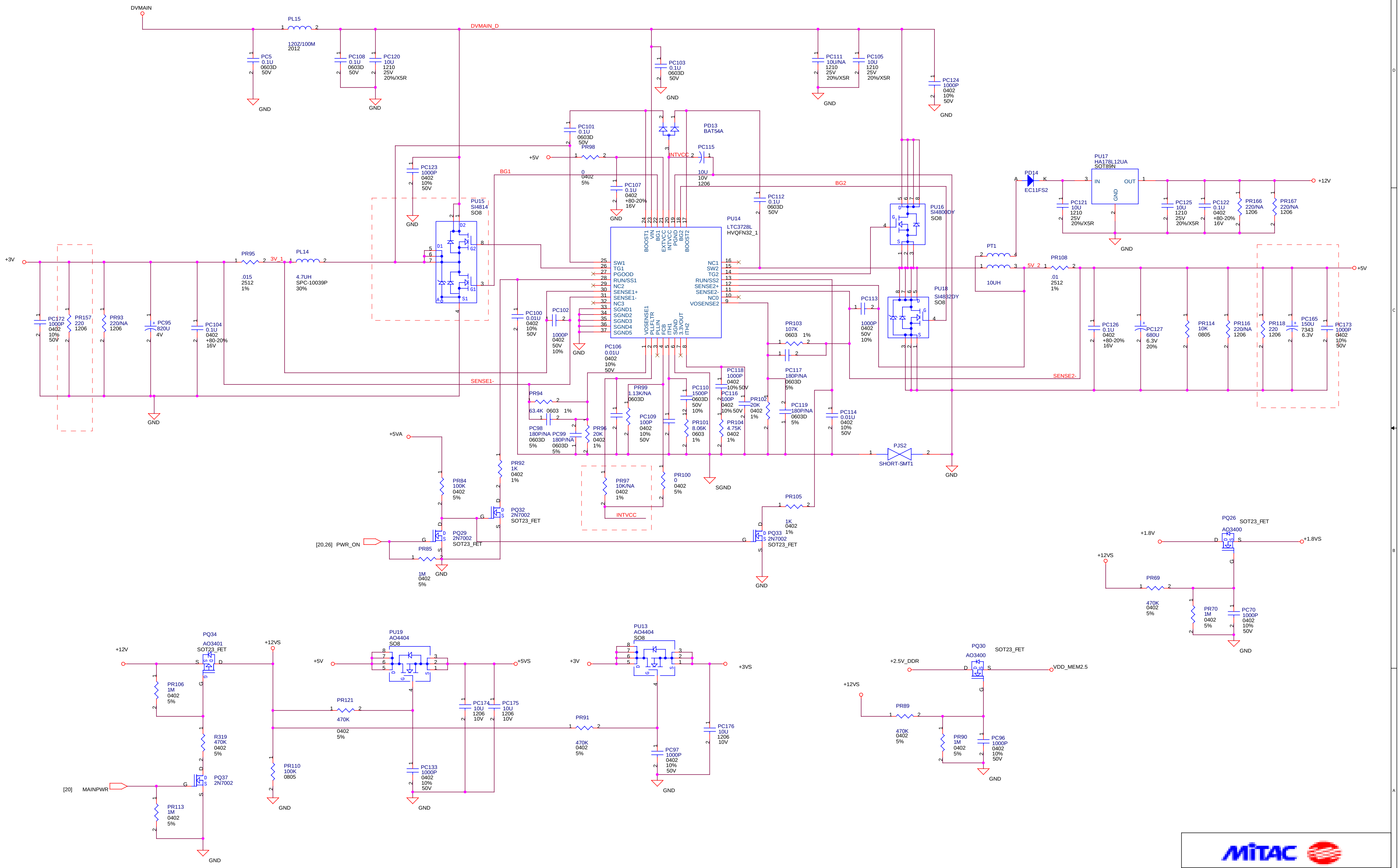
change from +5VA to +3VA

5V Resume Power

Title
Battery Connector

Size
Document Number **411682900001**
Rev R06

Date: Monday, April 12, 2004
Sheet 24 of 28

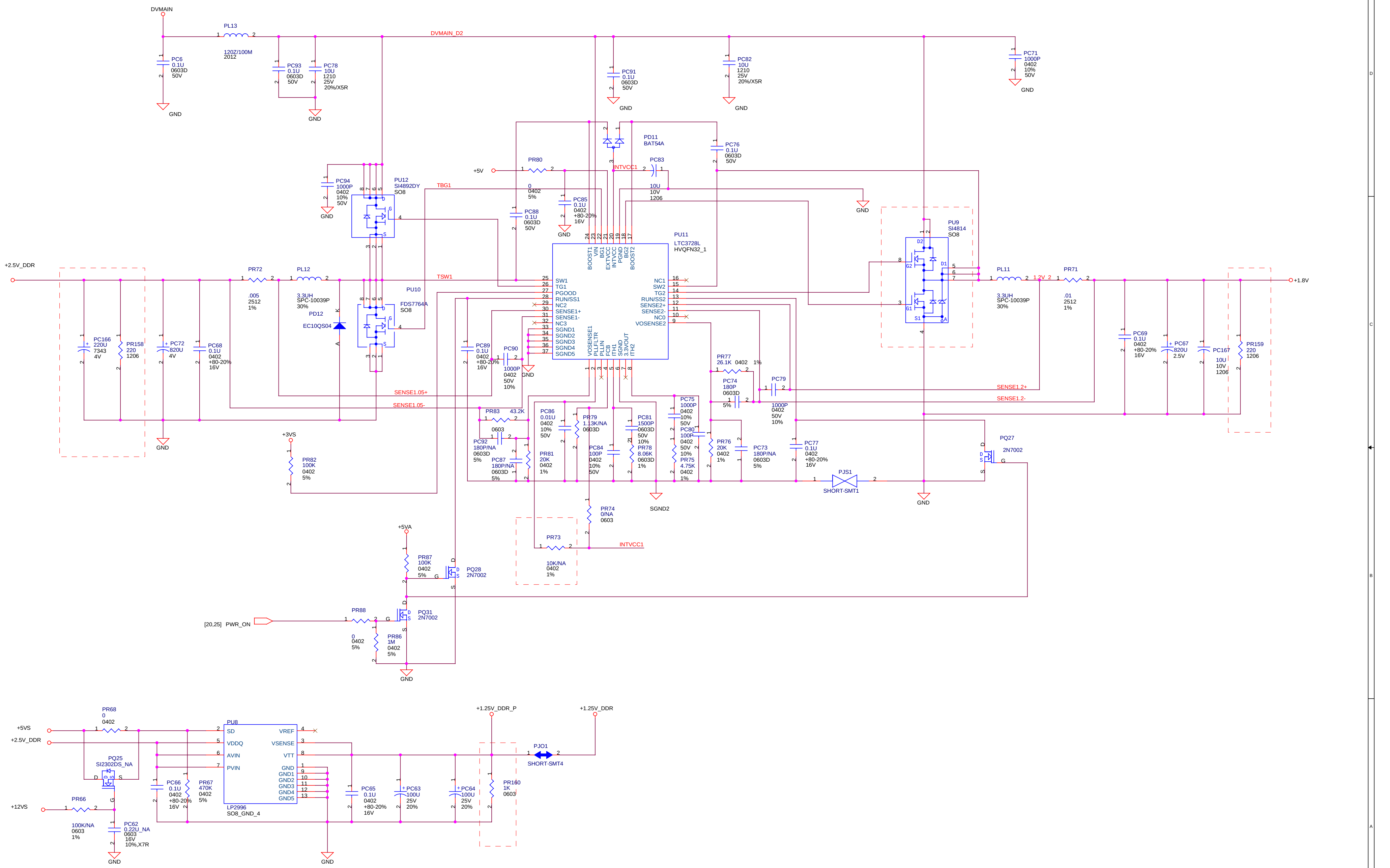

DVMAIN
PL15
120Z/100M
2012
DVMAIN_D
PC5 0.1U 0603D 50V
PC108 0.1U 0603D 50V
PC120 10U 1210 25V 20%/X5R
PC103 0.1U 0603D 50V
PC111 10U/NA 1210 25V 20%/X5R
PC105 10U 1210 25V 20%/X5R
PC124 1000P 0402 10% 50V
GND
PC101 0.1U 0603D 50V
PD13 BAT54A
PR98 0 0402 5%
+5V
INTVCC
PC115 10U 10V 1206
PC123 1000P 0402 10% 50V
BG1
BG2
PC107 0.1U 0402 +80-20% 16V
PC112 0.1U 0603D 50V
PU15 SI4814 SO8
PU16 SI4800DY SO8
PU14 LTC3728L HVQFN32_1
BOOST1 VIN BG1 EXTVCC INTVCC PGND BG2 BOOST2
SW1 TG1 PGOOD RUN/SS1 NC2 SENSE1+ SENSE1- NC3 SGND1 SGND2 SGND3 SGND4 SGND5
NC1 SW2 TG2 RUN/SS2 SENSE2+ SENSE2- NC0 VOSENSE2
VOSENSE1 PLLFLTR PLLIN FCB ITH1 SGND 3.3VOUT ITH2
PU17 HA178L12UA SOT89N
IN OUT GND
PD14 EC11FS2
+12V
PC121 10U 1210 25V 20%/X5R
PC125 10U 1210 25V 20%/X5R
PC122 0.1U 0402 +80-20% 16V
PR166 220/NA 1206
PR167 220/NA 1206
PT1
10UH
5V
PR108 .01 2512 1%
+5V
+3V
PR95 .015 2512 1%
3V
PL14 4.7UH SPC-10039P 30%
PC172 1000P 0402 10% 50V
PR157 220 1206
PR93 220/NA 1206
PC95 820U 4V
PC104 0.1U 0402 +80-20% 16V
PC100 0.01U 0402 50V
PC102 1000P 0402 50V 10%
PC106 0.01U 0402 10% 50V
PC113 1000P 0402 50V 10%
PU18 SI4832DY SO8
PR103 107K 0603 1%
PC117 180P/NA 0603D 5%
PC118 1000P 0402 10% 50V
PC116 100P 0402 10% 50V
PR102 20K 0402 1%
PC119 180P/NA 0603D 5%
PC114 0.01U 0402 10% 50V
PC110 1500P 0603D 50V 10%
PR99 1.13K/NA 0603D
PC109 100P 0402 10% 50V
PR101 8.06K 0603 1%
PR104 4.75K 0402 1%
SENSE1-
SENSE2-
PR94 63.4K 0603 1%
PC98 180P/NA 0603D 5%
PC99 180P/NA 0603D 5%
PR96 20K 0402 1%
PC126 0.1U 0402 +80-20% 16V
PC127 680U 6.3V 20%
PR114 10K 0805
PR116 220/NA 1206
PR118 220 1206
PC165 150U 7343 6.3V
PC173 1000P 0402 10% 50V
PJS2 SHORT-SMT1
SGND
+5VA
PR84 100K 0402 5%
PR92 1K 0402 1%
PQ32 2N7002 SOT23_FET
PR97 10K/NA 0402 1%
PR100 0 0402 5%
INTVCC
PR105 1K 0402 1%
PQ29 2N7002 SOT23_FET
PQ33 2N7002 SOT23_FET
[20,26] PWR_ON
PR85 1M 0402 5%
PQ26 SOT23_FET AO3400
+1.8V
+1.8VS
+12VS
PR69 470K 0402 5%
PR70 1M 0402 5%
PC70 1000P 0402 10% 50V
PQ34 AO3401 SOT23_FET
+12V
+12VS
PR106 1M 0402 5%
R319 470K 0402 5%
PQ37 2N7002
[20] MAINPWR
PR113 1M 0402 5%
PR110 100K 0805
PU19 AO4404 SO8
+5V
+5VS
PR121 470K 0402 5%
PC174 10U 1206 10V
PC175 10U 1206 10V
PC133 1000P 0402 10% 50V
PU13 AO4404 SO8
+3V
+3VS
PR91 470K 0402 5%
PC176 10U 1206 10V
PC97 1000P 0402 10% 50V
PQ30 AO3400 SOT23_FET
+2.5V_DDR
VDD_MEM2.5
+12VS
PR89 470K 0402 5%
PR90 1M 0402 5%
PC96 1000P 0402 10% 50V
D G S

MiTAC

Title
+12V,+5V,+3V,

Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 25 of 28


DVMAIN
PL13
120Z/100M
2012
DVMAIN_D2
PC6 0.1U 0603D 50V
PC93 0.1U 0603D 50V
PC78 10U 1210 25V 20%/X5R
PC91 0.1U 0603D 50V
PC82 10U 1210 25V 20%/X5R
PC71 1000P 0402 10% 50V
GND
PD11 BAT54A
PC76 0.1U 0603D 50V
PR80 0 0402 5%
+5V
INTVCC1
PC83 10U 10V 1206
PC85 0.1U 0402 +80-20% 16V
PC88 0.1U 0603D 50V
PC94 1000P 0402 10% 50V
PU12 SI4892DY SO8
TBG1
PU11 LTC3728L HVQFN32_1
BOOST1 VIN BG1 EXTVCC INTVCC PGND BG2 BOOST2
SW1 TG1 PGOOD RUN/SS1 NC2 SENSE1+ SENSE1- NC3 SGND1 SGND2 SGND3 SGND4 SGND5
NC1 SW2 TG2 RUN/SS2 SENSE2+ SENSE2- NC0 VOSENSE2
VOSENSE1 PLLFLTR PLLIN FCB ITH1 SGND 3.3VOUT ITH2
PU9 SI4814 SO8
+2.5V_DDR
PR72 .005 2512 1%
PL12 3.3UH SPC-10039P 30%
TSW1
PU10 FDS7764A SO8
PD12 EC10QS04
PL11 3.3UH SPC-10039P 30%
1.2V_2
PR71 .01 2512 1%
+1.8V
PC166 220U 7343 4V
PR158 220 1206
PC72 820U 4V
PC68 0.1U 0402 +80-20% 16V
PC89 0.1U 0402 +80-20% 16V
PC90 1000P 0402 50V 10%
PC69 0.1U 0402 +80-20% 16V
PC67 820U 2.5V
PC167 10U 10V 1206
PR159 220 1206
SENSE1.05+
SENSE1.05-
SENSE1.2+
SENSE1.2-
PR77 26.1K 0402 1%
PC74 180P 0603D 5%
PC79 1000P 0402 50V 10%
PR83 43.2K 0603
PC92 180P/NA 0603D 5%
PC87 180P/NA 0603D 5%
PR81 20K 0402 1%
PC86 0.01U 0402 10% 50V
PR79 1.13K/NA 0603D
PC84 100P 0402 10% 50V
PC81 1500P 0603D 50V 10%
PR78 8.06K 0603D 1%
PC75 1000P 0402 10% 50V
PC80 100P 0402 50V 10%
PR75 4.75K 0402 1%
PR76 20K 0402 1%
PC73 180P/NA 0603D 5%
PC77 0.1U 0402 +80-20% 16V
PQ27 2N7002
PJS1 SHORT-SMT1
SGND2
+3VS
PR82 100K 0402 5%
PR74 0/NA 0603
PR73 10K/NA 0402 1%
INTVCC1
+5VA
PR87 100K 0402 5%
PQ28 2N7002
PQ31 2N7002
PR88 0 0402 5%
PR86 1M 0402 5%
[20,25] PWR_ON
PR68 0 0402
+5VS
+2.5V_DDR
PQ25 SI2302DS_NA
PR66 100K/NA 0603 1%
+12VS
PC62 0.22U_NA 0603 16V 10%,X7R
PC66 0.1U 0402 +80-20% 16V
PR67 470K 0402 5%
PU8 LP2996 SO8_GND_4
SD VDDQ AVIN PVIN VREF VSENSE VTT GND GND1 GND2 GND3 GND4 GND5
+1.25V_DDR_P
+1.25V_DDR
PJO1 SHORT-SMT4
PC65 0.1U 0402 +80-20% 16V
PC63 100U 25V 20%
PC64 100U 25V 20%
PR160 1K 0603

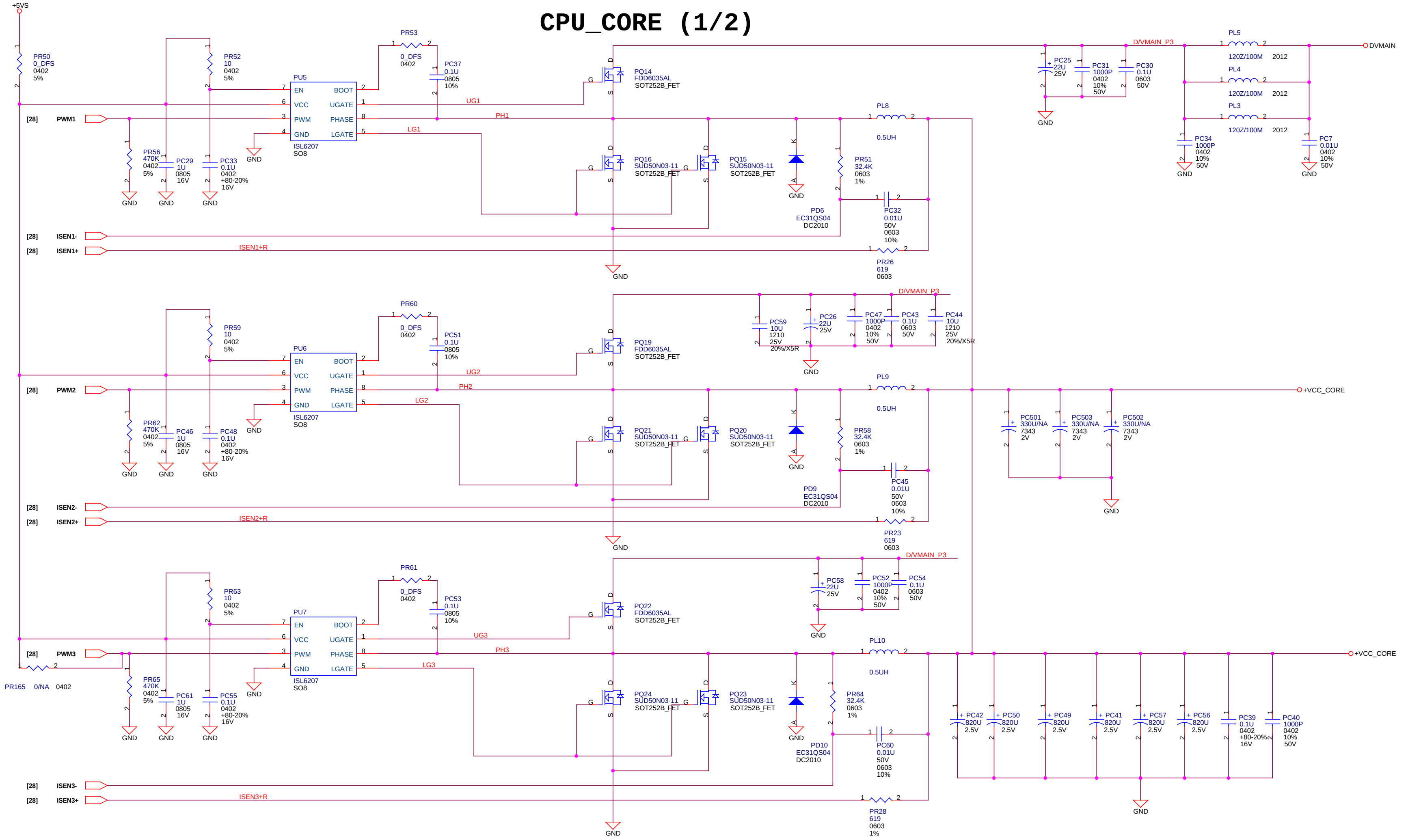
MiTAC

Title
+2.5V,1.25V,1.8VS

Size	Document Number	Rev
	411682900001	R06

Date: Monday, April 12, 2004 Sheet 26 of 28

CPU_CORE (1/2)


+5VS
PR50 0_DFS 0402 5%
PR52 10 0402 5%
PR53 0_DFS 0402
PC37 0.1U 0805 10%
PU5 ISL6207 SO8
EN VCC PWM GND BOOT UGATE PHASE LGATE
UG1
PH1
LG1
[28] PWM1
PR56 470K 0402 5%
PC29 1U 0805 16V
PC33 0.1U 0402 +80-20% 16V
GND
PQ14 FDD6035AL SOT252B_FET
PQ16 SUD50N03-11 SOT252B_FET
PQ15 SUD50N03-11 SOT252B_FET
PD6 EC31QS04 DC2010
PL8 0.5UH
PR51 32.4K 0603 1%
PC32 0.01U 50V 0603 10%
PR26 619 0603
[28] ISEN1-
[28] ISEN1+
ISEN1+R
D/VMAIN_P3
PC25 22U 25V
PC31 1000P 0402 10% 50V
PC30 0.1U 0603 50V
PL5 120Z/100M 2012
PL4 120Z/100M 2012
PL3 120Z/100M 2012
DVMAIN
PC34 1000P 0402 10% 50V
PC7 0.01U 0402 10% 50V
PR59 10 0402 5%
PR60 0_DFS 0402
PC51 0.1U 0805 10%
PU6 ISL6207 SO8
UG2
PH2
LG2
[28] PWM2
PR62 470K 0402 5%
PC46 1U 0805 16V
PC48 0.1U 0402 +80-20% 16V
PQ19 FDD6035AL SOT252B_FET
PQ21 SUD50N03-11 SOT252B_FET
PQ20 SUD50N03-11 SOT252B_FET
PC59 10U 1210 25V 20%/X5R
PC26 22U 25V
PC47 1000P 0402 10% 50V
PC43 0.1U 0603 50V
PC44 10U 1210 25V 20%/X5R
PL9 0.5UH
+VCC_CORE
PC501 330U/NA 7343 2V
PC503 330U/NA 7343 2V
PC502 330U/NA 7343 2V
PR58 32.4K 0603 1%
PD9 EC31QS04 DC2010
PC45 0.01U 50V 0603 10%
PR23 619 0603
[28] ISEN2-
[28] ISEN2+
ISEN2+R
PR63 10 0402 5%
PR61 0_DFS 0402
PC53 0.1U 0805 10%
PU7 ISL6207 SO8
UG3
PH3
LG3
[28] PWM3
PR165 0/NA 0402
PR65 470K 0402 5%
PC61 1U 0805 16V
PC55 0.1U 0402 +80-20% 16V
PQ22 FDD6035AL SOT252B_FET
PQ24 SUD50N03-11 SOT252B_FET
PQ23 SUD50N03-11 SOT252B_FET
PC58 22U 25V
PC52 1000P 0402 10% 50V
PC54 0.1U 0603 50V
PL10 0.5UH
PR64 32.4K 0603 1%
PD10 EC31QS04 DC2010
PC60 0.01U 50V 0603 10%
PR28 619 0603 1%
[28] ISEN3-
[28] ISEN3+
ISEN3+R
PC42 820U 2.5V
PC50 820U 2.5V
PC49 820U 2.5V
PC41 820U 2.5V
PC57 820U 2.5V
PC56 820U 2.5V
PC39 0.1U 0402 +80-20% 16V
PC40 1000P 0402 10% 50V
+VCC_CORE

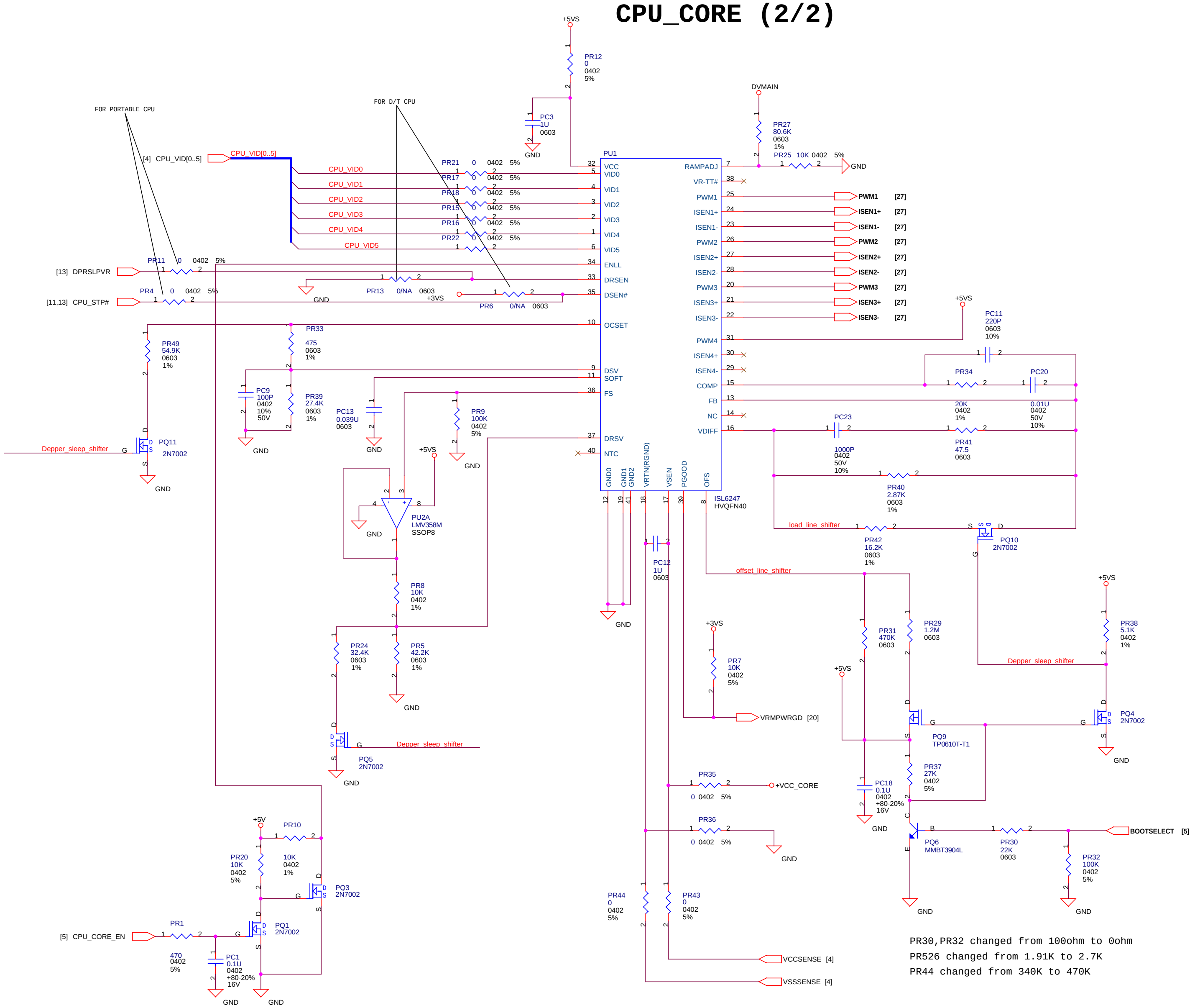
MiTAC

Title
CPU_CORE1

Size | Document Number 411682900001 | Rev R06

Date: Monday, April 12, 2004 | Sheet 27 of 28

CPU_CORE (2/2)


+5VS
PR12 0 0402 5%
PC3 1U 0603
GND
DVMAIN
PR27 80.6K 0603 1%
PR25 10K 0402 5%
FOR PORTABLE CPU
FOR D/T CPU
[4] CPU_VID[0..5]
CPU_VID[0..5]
CPU_VID0
CPU_VID1
CPU_VID2
CPU_VID3
CPU_VID4
CPU_VID5
PR21 0 0402 5%
PR17 0 0402 5%
PR18 0 0402 5%
PR15 0 0402 5%
PR16 0 0402 5%
PR22 0 0402 5%
PU1
VCC
VID0
VID1
VID2
VID3
VID4
VID5
ENLL
DRSEN
DSEN#
OCSET
DSV
SOFT
FS
DRSV
NTC
GND0
GND1
GND2
VRTN(RGND)
VSEN
PGOOD
OFS
RAMPADJ
VR-TT#
PWM1
ISEN1+
ISEN1-
PWM2
ISEN2+
ISEN2-
PWM3
ISEN3+
ISEN3-
PWM4
ISEN4+
ISEN4-
COMP
FB
NC
VDIFF
ISL6247
HVQFN40
PWM1 [27]
ISEN1+ [27]
ISEN1- [27]
PWM2 [27]
ISEN2+ [27]
ISEN2- [27]
PWM3 [27]
ISEN3+ [27]
ISEN3- [27]
PR11 0 0402 5%
[13] DPRSLPVR
PR4 0 0402 5%
[11,13] CPU_STP#
PR13 0/NA 0603
PR6 0/NA 0603
+3VS
PR33 475 0603 1%
PR49 54.9K 0603 1%
PC9 100P 0402 10% 50V
PR39 27.4K 0603 1%
PC13 0.039U 0603
PR9 100K 0402 5%
Depper_sleep_shifter
PQ11 2N7002
PU2A LMV358M SSOP8
PR8 10K 0402 1%
PR24 32.4K 0603 1%
PR5 42.2K 0603 1%
PQ5 2N7002
+5V
PR10 10K 0402 1%
PR20 10K 0402 5%
PQ3 2N7002
PR1 470 0402 5%
[5] CPU_CORE_EN
PQ1 2N7002
PC1 0.1U 0402 +80-20% 16V
PC11 220P 0603 10%
PR34 20K 0402 1%
PC20 0.01U 0402 50V 10%
PC23 1000P 0402 50V 10%
PR41 47.5 0603
PR40 2.87K 0603 1%
load_line_shifter
PR42 16.2K 0603 1%
PQ10 2N7002
PC12 1U 0603
offset_line_shifter
PR31 470K 0603
PR29 1.2M 0603
PR38 5.1K 0402 1%
PR7 10K 0402 5%
VRMPWRGD [20]
PQ9 TP0610T-T1
PQ4 2N7002
PR37 27K 0402 5%
PC18 0.1U 0402 +80-20% 16V
PR35 0 0402 5%
+VCC_CORE
PR36 0 0402 5%
PQ6 MMBT3904L
PR30 22K 0603
BOOTSELECT [5]
PR32 100K 0402 5%
PR44 0 0402 5%
PR43 0 0402 5%
VCCSENSE [4]
VSSSENSE [4]

PR30,PR32 changed from 100ohm to 0ohm
PR526 changed from 1.91K to 2.7K
PR44 changed from 340K to 470K

Title
CPU_CORE2
Size Document Number 411682900001 Rev R06
Date: Monday, April 12, 2004 Sheet 28 of 28

Reference Material

❖ Intel Pentium 4 Processor Specifications	*Intel,INC*
❖ SiS M661FX (Host Memory Controller)	*SiS,INC*
❖ SiS963L(MuTIOL®Media I/O South Bridge)	*SiS,INC*
❖ Frequency Generator ICS952007	*ICS,INC*
❖ 8599 Hardware Engineering Specification	*Technology.Corp./MiTAC*

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